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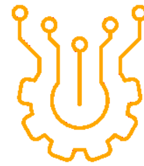

TEILVORHABEN

Technologien der Aufbau- und Verbindungs-technik für Photonik und Mikroelektronik

Förderkennzeichen: 16ESE0352
Laufzeit: 01.05.2019 bis 30.10.2022*
(* 6-monatige KN Verlängerung)

im Rahmen des Gesamtvorhabens

APPLAUSE

Advanced packaging for photonics, optics and electronics for low cost manufacturing in Europe

Call: ECSEL 2018-1 Innovation Action

Schlussbericht

Berichtszeitraum: 01.05.2019 bis 31.10.2022

Fraunhofer IZM

Partner:	Kontaktperson:
Fraunhofer IZM Gustav-Meyer-Allee 25 13355 Berlin	Dr. Charles-Alix Manier Charles-alix.manier@izm.fraunhofer.de Tel.: +49 30 46403 -612 Dr. Hermann Oppermann hermann.oppermann@ izm.fraunhofer.de Tel.: +49 30 46403 -163

Schlussbericht

zum Teilvorhaben:

Technologien der Aufbau- und Verbindungstechnik für Photonik und Mikroelektronik

Zuwendungsempfänger: Fraunhofer-Gesellschaft für ihr Institut

- **Fraunhofer-Institut für Zuverlässigkeit und Mikrointegration IZM**

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Teil I: Zusammenfassung

Aufzählung der wichtigsten wissenschaftlich-technischen Ergebnisse und anderer wesentlicher Ereignisse (maximal 1/2 Seite!).

Im Lauf des Projektes sind die Arbeiten nach Auslegung von Spezifikationen (WP2) und Design (WP3) mit Projekt-Partners um einzelnen Prozess-entwicklungen (WP4) und Überführung in einer Prozesskette für Packaging (WP5) herum drei anvisierten Applikationen gelenkt worden:

- Applikation 2 - Kostengünstige Wärmebildgeräte,
- Applikation 3 - Passive Faserausrichtung für Single-Mode-Transceiver und
- Applikation 4 - Herzüberwachungssystem

Arbeiten am Fraunhofer IZM auf Prozesse sind in Shortloops und deren Kombinationen in gesamten Prozessabläufen (WP4) durchgeführt worden, um die Überführung in WP5 (Packaging) zu gewährleisten.

Bei der Applikation 2 sind die Prozessabläufe für die Vorbereitung von Device Wafer (Sensor) und Silizium Cap Wafer (Deckel) vollständig abgeschlossen worden und Packaging führten letztendlich zur Wafer Level hermetischen Verkapselung unter Vakuum sowohl von Mikrobolometer Materialen von der Firma IDEAS (Norwegen) über seinen Partner NNFC (Süd-Korea) bereitgestellt, als auch von MEMS-basierten Pirani Sensoren von Fraunhofer IMS (Fertigung) und USN (Design und Charakterisierung) (University South Norway, Norwegen). Hiermit wurde in 2023 eine Vakuum Level von 10^{-1} mbar nachgewiesen. Die Wafer Level Verkapselung-Ausbeute (Yield) wurde bei über 95% abgeschätzt. Bond-Tests anhand flachen Germanium-Lid auf Silizium-Frame erwiesen sich auf Chip-level nicht zufriedenstellend, mit Teilbruch oder Riss-Bildung in Si-Stegen (Bond auf Silizium Frame) oder in Ge (Bond auf flächigem Si) bei AuSn-Bonden auf Silizium und belegt eine Full-Silicon-Packaging Ansatz als geeigneter für Wafer Level Bonding.

Im Fall der Applikation 3 ist die Fabrikation eines 3D-Silizium Bench inkl. Vielzahl an Sub-Varianten/Testvehicles mittels Silizium-Strukturierung abgeschlossen worden. Die Flip chip Verfahren sind für Integration der Laser Chips durchgeführt worden. Zusätzlich sind optische Bauelemente (Linse, Isolator) darauf montiert worden (nicht als vorgesehen Arbeitstask, Task BESI-AT). 3D Submounts (Silicon und Mold) sind auch an involvierten Partner (BESI Austria) für die präzise Assemblierung der optischen Teile (Die-Attach des Laser Die, Einbau Optik-Elementen) zur Verfügung gestellt worden.

Im Rahmen der Applikation 4 ist der Flex-basierte Integration anhand funktionaler Teile erfolgreich durchgeführt worden. Hierbei sind High Density Polyimid basierte Flex Substrate hergestellt worden, worin bzw. worauf elektronische Bauelemente in unterschiedliche AVT (Flip chip und SMT) aufgebaut worden sind und in einem TPU flexible Material eingegossen. Nach korrekter Einbettung sind die Aussenkontakte finalisiert worden. Der Impakt vom Covid-19 und sanitären Gegenmaßnahmen ließen sich durch starkgebremsten Arbeit-fortschritte negativ spüren, insbesondere bei Prozessentwicklungen, wofür Home-Office nicht infrage kommen kann.

Der beiliegende Bericht fasst die unternommenen Arbeiten für die Gesamtzeitfenster des Projektes zusammen. Der folgende Sachbericht ist wie bei den Zwischenberichten auf Englisch weiterverfasst worden.

2) Vergleich des Stands des Vorhabens mit der ursprünglichen (bzw. mit Zustimmung des ZG geänderten) Arbeits-, Zeit- und Kostenplanung.

☒* Das Vorhaben liegt im Wesentlichen innerhalb der ursprünglichen (bzw. mit Zustimmung des ZG geänderten) Arbeits-, Zeit- und Kostenplanung.

☐* Eine Anpassung des Arbeitsplans wird erforderlich (Erläuterung erforderlich).

Nein

☒* Es sind zeitliche Verzögerungen aufgetreten (Erläuterung erforderlich).

Die sanitäre Lage hat erheblichen Weiterauswirkungen auf die Projekt-Arbeiten gehabt (beschränkten Personal-Anwesenheit, Krankmeldung vom Personal, Verspätungen in Wartungen und Services, etc). Aufgrundessen ist das Projekt auf 42 Monate (M412 = Okt22) nach EU- sowie nationaler Bewilligungen kostenneutral verlängert worden.

☐* Es sind Mehr- oder Minderausgaben aufgetreten (Erläuterung erforderlich).

Nein

3) Haben sich die Aussichten für das Erreichen der Ziele des Vorhabens innerhalb des angegebenen Berichtszeitraums gegenüber dem ursprünglichen Antrag geändert (Begründung)?

☒* Die Aussichten für das Erreichen der Ziele des Vorhabens haben sich gegenüber dem Zeitpunkt der Antragstellung nicht verändert.

☐* Die Aussichten für das Erreichen der Ziele des Vorhabens haben sich geändert (Erläuterung erforderlich).

Die Aussichten haben sich im Jahr 2022 nicht geändert, dennoch:

Bei Applikation 2 ist die Bereitstellung von funktionalen Sensor Device Wafer durch Use Case Leader (MEMS Bolometer, IDEAS, Norwegen) letztendlich gescheitert. Sein externe Subcontractor war nicht in der Lage Sensoren zu finalisieren, die für das Projekt als Prozess- und Funktionsdemonstration vorgesehen waren. Die Arbeiten blieben unzufriedenstellend in dem Fall auf nicht-funktionalen / ShortLoop Mikrobolometer, ohne möglichen Nachweis auf Nieder-Vakuum Verkapselung (Niedervakuum notwendig für MEMS Funktion). Als Gegenmaßnahme wurde ein Pirani-Sensor von Fraunhofer IMS mittels Wafer Level Packaging am Fraunhofer IZM mit Silizium-Cap in Vakuum verkapselt, und hiermit das resultierende eingekapselte Vakuum in Zusammenarbeit mit USN / Norwegen (Pirani Design und Charakterisierung) evaluiert.

Die Applikation 3 litt der Rücktritt des Use Case Leaders (Dustphotonic, Israel) aus dem Konsortium. Der passive Aufbau der Optik-Teilen (Linse, Isolator, Faser) auf dem Silizium Bench für vollständige Assemblierung eines Transmitter-Submodule sollte vom Partner BESI-AT übernommen werden (komplette Assembly sollte für das 3D Mold Substrate gemäß Projekt ohnehin dort erfolgen), blieb aber bei Projekt-Abschluss ausstehend. Die in 2023 von BESI-

AT vervollständigt-aufgebauten Submounts erwiesen sich lediglich als nicht genug präzis-assembliert.

Bei der Applikation 4 sind die funktionalen Chips (IC, Flash Memory) nicht im Flex-Substrate eingebettet, sondern auf Flex-Substrate geflippt und anschliessend ist der Flip chip Flex in flexibles Material für die Patch-Herstellung eingebettet worden. Hintergrund war einerseits der hohe Risk bei rückdünnen von hoch integrierten Prozessor MUSEIC chips von IMEC-NL kombiniert an kanppe und verzögerte Verfügbarkeit von funktionalen einzel-chips, um dies vorzutesten. Anderseits die Flash Memory Chips hätten höchstwahrscheinlich das thermische Budget des Gesamtprozesses nicht überstanden.

4) Sind inzwischen von dritter Seite FuE-Ergebnisse bekannt geworden, die für die Durchführung des Vorhabens relevant sind?

☒* Nein

☐* Ja (Erläuterung erforderlich)

5) Sind oder werden Änderungen in der Zielsetzung notwendig?

☒* Nein

☐* Ja (Erläuterung erforderlich)

6) Jährliche Fortschreibung des Verwertungsplans. Diese soll, soweit im Einzelfall zutreffend, Angaben zu folgenden Punkten enthalten:

☐* Im Berichtszeitraum wurden auf Basis der Ergebnisse des Vorhabens Schutzrechte angemeldet, erteilt oder eine Anmeldung vorbereitet (Erläuterung erforderlich).

Nein.

☐* Im Berichtszeitraum sind Änderungen der wirtschaftlichen Erfolgsaussichten nach Projektende gegenüber der Darstellung im Antrag aufgetreten (Erläuterung erforderlich).

Nein.

☐* Im Berichtszeitraum sind Änderungen der wissenschaftlichen und/oder technischen Erfolgsaussichten nach Projektende gegenüber der Darstellung im Antrag aufgetreten (Erläuterung erforderlich).

Nein.

☐* Im Berichtszeitraum sind Änderungen der wissenschaftlichen und wirtschaftlichen Anschlussfähigkeit gegenüber der Darstellung im Antrag aufgetreten (Erläuterung erforderlich).

Nein.

Part II: Technical report

WP1 Management

Task 1.1 Technical Coordination

Fraunhofer IZM leaded work package 5 and coordinated the cooperation between the partners within this work package. Fraunhofer IZM supported the overall project coordination by ICOS (BE) and Spinverse (FI) regarding the implementation of the application scenarios and technical support.

Work related to project management was concentrated on participation to monthly TCC online meetings (Technical coordination committee) and following developments in other Work Packages especially WP3 and WP4, since most of works had to be transferred into WP5 based on progresses and lessons learned in WP4. For the UCs wherein Fraunhofer IZM was directly involved, collaboration dealed directly inside the UC clusters and with respective UC owners.

WP2 Requirements and Specifications

Task 2.2 Requirements and specifications for UC2 (Low cost thermal imaging systems)

In UC2, Fraunhofer IZM was contributor for wafer level packaging of a low-cost thermal image system, owned by the UC owner/leader IDEAS (Norway). For vacuum packaging of IR camera, a lid was developed with a transparent window and bonded to a bolometer chip at wafer level and hermetically sealed.

Different capping structures (Figure 1) and window materials were first compared and validated against the objectives. Due to cost constraints and lifetime expectations a highly transparent silicon (HiTSi) window has been retained instead of Germanium as originally planned.

For longer lifetime the variant based on silicon (Si) frame should provide a large vacuum capacity and allows the deposition of getter material. Depending on the cap topology, the achievable internal volume differs largely as well as internal volume-to-surface ratio, which might have some influences on the functionality of the MBA. Also, double (upper sketches, “Ge-Window” and “Si window”) or single (lower sketches, “Si monolithic” and “Si flat lid”) seal bonding were considered depending on the topology, these being reflected in the complexity of the corresponding process flow.

At Task.2.2 level, it was foreseen to compare a Ge-based and a Si-based window topology regarding the sealing feasibility and reliability. Some questions were clarified, regarding the bolometer provided by IDEAS in the way of delivery form, i.e. In other terms how the bolometer wafer technically looks like, especially regarding protection of the bolometer structures vs. Processing compatibility.

For cap fabrication, different suppliers were contacted, with focus on European collaboration, for silicon and AR coating. Two possible suppliers for the Si Wafer for providing the lid were identified, the first one in Germany (with also the possibility of deposition of the required Anti-Reflective Coating), and the other one in Denmark (only the base material, drawback: ARC should be applied by another external supplier).

The feasibility of incorporating an AR coating inside the structured Si monolithic cap was also considered (AR coating being not in the consortium capabilities and will be subcontracted to third one). However, the inner AR coating was not implemented and withdrawn, to limit complexity and save process time as debated with UC2 Owner IDEAS.

An industrial German AR supplier for deposition on 200mm wafer could be also identified for the wavelength range, i.e. for Si substrate in the LWIR range, and for 200 mm wafers, the main constraint regarding WLP at FhG-IZM. The coating was tested on monitor wafers regarding compliancy with process flow (WP4, 5 and WP6).

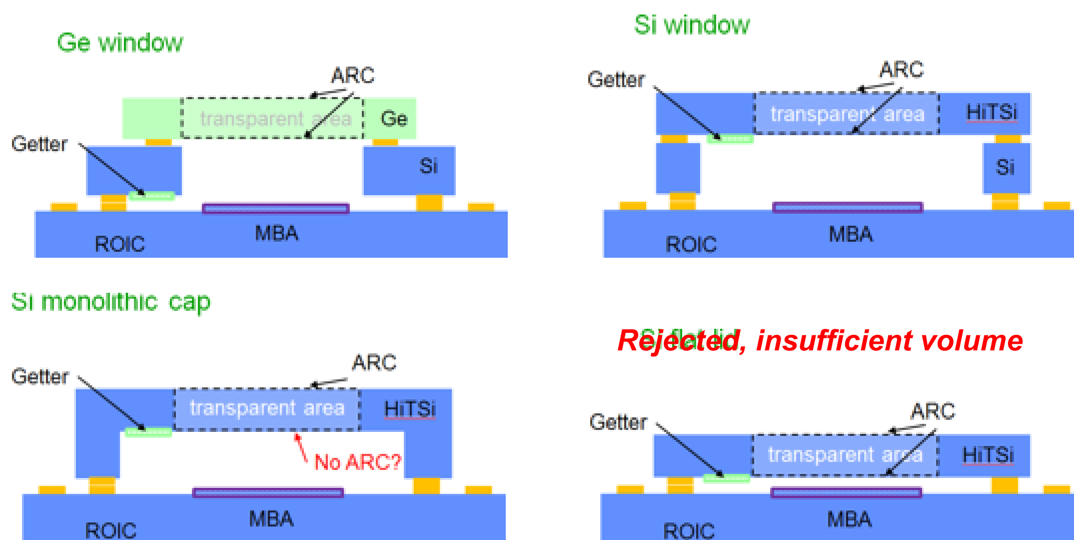


Figure 1: Cap topologies considered for the WLP of the microbolometer, based on Germanium or/and Silicon window material

On the side of wafer level packaging, the main requirements as defined/revised can be globally summarized as follow:

- Cap thickness:
  A 300 µm silicon thickness has been chosen for roof thickness of the monolithic silicon cap and Silicon Lids, since providing mechanical robustness (in view of advanced packaging, especially Die Attach and Molding at consortium partner sides) and a minor bending of few micrometers (based on mechanical estimation of pressure difference), which should be measurable but also without any impact on optical aspects (transmission and distortion).

- Silicon Body thickness:
  Total thickness of monolithic silicon cap will be in the range of 650 µm as from provider, and the silicon frame in the range of 700 µm.

- Cap size:
  The cap size and sealing ring location should permit a 500 µm clearance to the pad ring with the wire bond contacts.

- Bond rings:
  1 Gold-based (gold on one side and gold-tin on the other side) sealing bond ring of ca. 10 µm total thickness have been selected to enable AuSn soldering. The gold-tin ring will be applied on bolometer side and silicon lids, the monolithic cap and frame with gold rings.

2 Since the IDEAS Bolometer might only be provide with a very thin top oxide of 20 nm, the seal ring should not lay over critical areas where last metal is only covered by this top oxide. Discussed and fixed in coordination with IDEAS.

- Anti-reflective coating:
  Anti-reflective coating for LWIR spectrum is only applied on the outer side of the capping parts, as discussed with end user / use case leader. The coating will be protected during wafer level processing, to avoid any damages / scratches during handling and process phases.

- Getter:
  A getter will be applied inside the package and provided by subcontractor. Interface to subcontractor (wafer alignment, clearances, size maximized accordingly) has been here clarified.

The device/Bolometer wafers were provided with Semi-Notch (Fraunhofer IMS) and Flat (IDEAS with its subcontractor NNFC/South Korea). In this case a flat-to-notch adapter has been required to allow processing on the needed stations of the technological park of Fraunhofer IZM.

In view of hermetic packaging, special countermeasures were implemented in the process flow at Fraunhofer IZM.

The requirements were synthesized with UC contributors in the EU Deliverable D2.2: Requirements and specifications for UC2: Low cost thermal imaging system.

Task 2.3 Requirements and specifications for UC3 (Passive fibre alignment for single-mode transceivers)

The use case 3 pursues the goal of fabricating a single mode transceiver. Within the use case, intention was to develop a process for high precision bonding of EML components onto an optical bench to allow for passive fibre alignment relative to the EML/laser source. The silicon bench comprises 4 channels à 1.6mm Pitch, which should fit within the transceiver board (Figure 2).

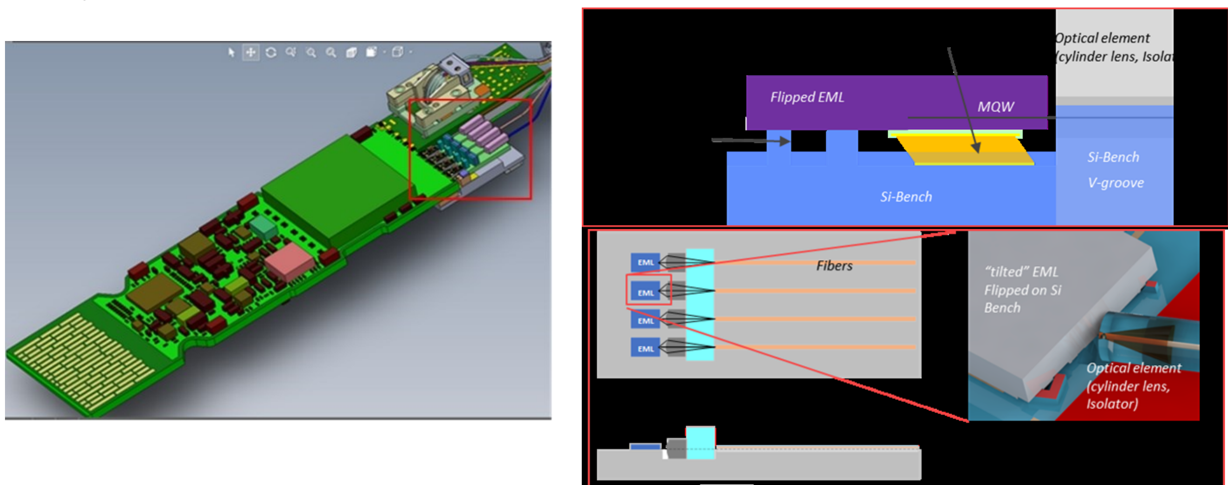


Figure 2. 3D-view of the transceiver of DPH with the 4Channel submount (in red square), Schematic of the for the passive alignment of the EML; basic sketch of the Si-bench with self-aligned EML and optical components (right)

The requirements are especially focused on the side of Fraunhofer IZM on the passive alignment and all the required geometries. The silicon bench was first drafted using CAD software to better apprehend the needed 3D geometry (Figure 3).

The results of the optical simulation performed by DustPhotonics with the arrangement of the single optical elements “cylindrical lens + Isolator + Fiber” were included in the 3D model, in order to derive the entire required geometry of the silicon bench and all the needed relative spaces and depths.

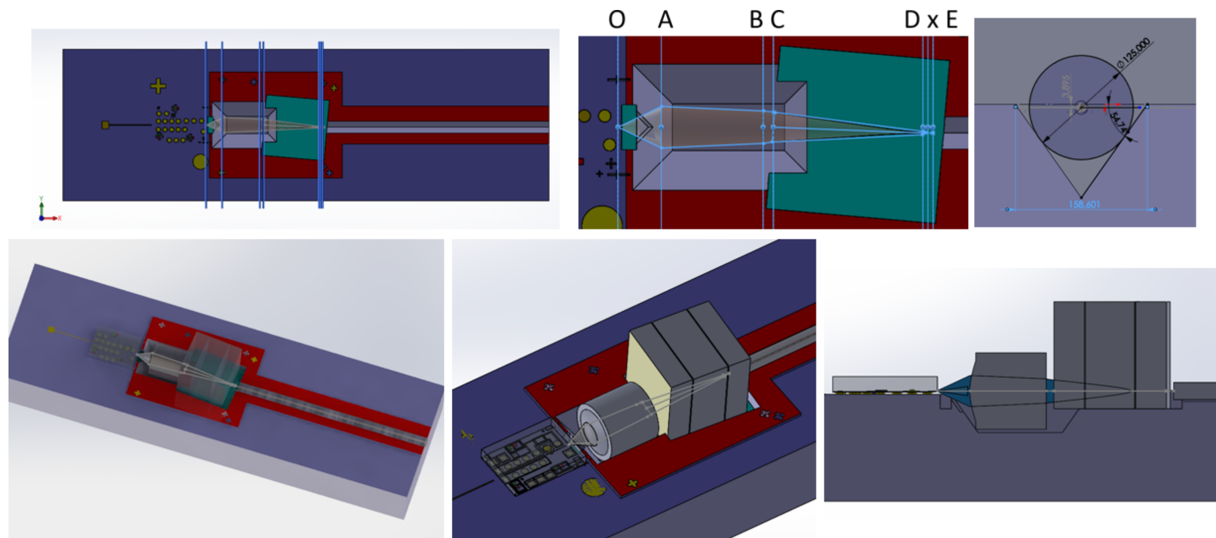


Figure 3: 3D-CAD layout of the Unit Cell (1x Channel) of the silicon optical bench with EML device flipped and metallically bonded to Si bench, cylindrical lens, isolator and Fiber with recesses/v-grooves and fiducials (HF routing on silicon not represented)

On the side of precise flip chip assembly, two different approaches to achieve precise passive bonding of the laser in flip chip were at this level/task considered:

1. Liquid solder assisted self-alignment of EML devices to the silicon bench with mechanical stops. Lateral stoppers and v-groove must be fabricated in a same mask so that they are defined in a same lithography process, bypassing any mask-to-mask (or design layer to design layer) shift caused by mask registration/alignment.

2. High precision thermocompression bonding with electroplated gold bumps onto the silicon bench. The Assembly is to be performed using a flip chip bonder presently available at FhG-IZM. The bonder has been purchased some months ago and according to the manufacturer allows assembly with a bonding precision down to 0.5 µm.

Two different variants of the EML device were foreseen and conceived/co-designed with the laser fabricant of the consortium ALMAE (France):

- straight, i.e. the laser beam output is perpendicular to the facet,
- 7° tilted, the laser source is tilted from the facet by a 7° angle to avoid back reflection into the chip, as explorative work.

Where both are intended to be used for solder self-alignment as well as for thermocompression bonding. This boundary rises the number of base layouts to the quantity of 4 (2x different flip chip technologies, 2x chip variants), to be conceived and included in the Wafer layout.

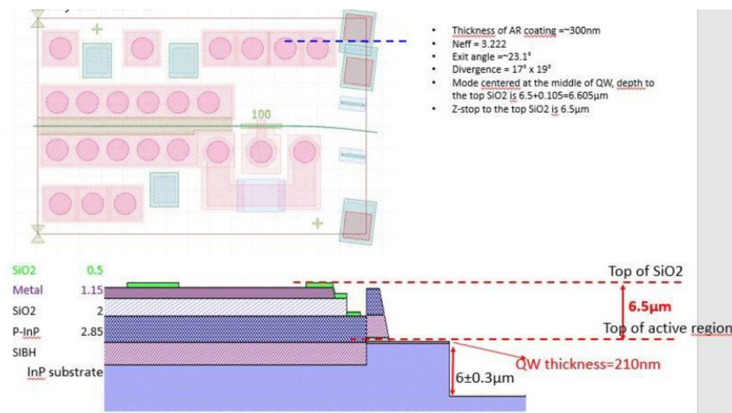


Figure 4. Depth definition of the recesses in the InP EML devices by ALMAE

FhG IZM has also jointly worked with ALMAE, France (InP laser provider) and Dustphotonics (first Use Case Leader, Israel) on design features so to implement the needed mechanical stoppers into the EML (definition of the etching depths in InP, sizing of recesses for z-Spacer and X/Y stoppers, fiducials in MQW optical layer) and the silicon bench. A sketch in cross-section from ALMAE recapitulates the technical feasible layer stack of the InP (Figure 4).

A keep out distance of the pads to the facet was also considered in chip version 2. Effectively it was found that the Antireflection Coating is being applied over the pads by the deposition process and the pads are not far enough from facet, affecting the solderability of the pads for self-alignment. The IOs of the InP FC component were terminated with TiPtAu (Au ~ 1µm).

The 2 chip versions further increased by 8 the number of base layouts needed (2x different flip chip technologies, 2x chip variants (straight and tilt), 2 chip versions/generations)

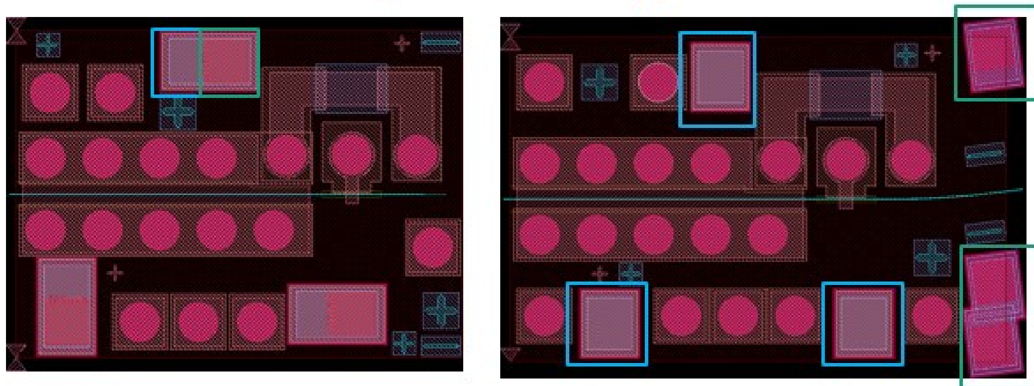


Figure 5: Overview of both GDS Layouts of ALMAE's EML devices (straight EML, left, and Tilt EML, right), devices size 500x685 µm und 500x780µm

The relative optical arrangement of the different elements (Figure 5) were fixed at M10, and implemented in the design (WP3) of the silicon bench. Several extensive iterations for layouting of the silicon bench were necessary, taking into consideration the foreseen sizes of the needed single elements / free space optics (lens + isolator) and the glass SM fibers as of D2.3 (see Table 1).

The EU deliverable D2.3 ("Requirements and specifications for UC3: Passive fibre alignment for single mode transceivers") summarized the relevant Use Case requirements.

Lens:	Isolator	Fiber:
• Diameter: 500 µm outer diameter, nominal • V-groove width: 617.9 µm (without compensation of silicon oxide thickness for Bench passivation) • V-Groove depth: at least 250 µm	• Footprint Size: 700x734 µm • Groove depth at least >73µm (vertical beam diameter at this interface)	• Diameter: 125 µm outer diameter, nominal • V-Groove Width: 158.6 µm (without compensation of silicon oxide thickness for Bench passivation)

Table 1: Free optic elements for UC3 from DustPhotonics

Task 2.4 Requirements and specifications for UC4 (Cardiac monitoring patch)

Fraunhofer IZM has provided specifications within the consortium for the design of the high-density flex with the embedded ICs as well as the stretchable substrate. The specifications included amongst others the required and expected thickness for dies to be embedded and the material stack layup for the flex and stretchable circuits. Furthermore, possible lateral dimensions of routing lines, vias and electrical and mechanical properties of the materials were fixed.

The layout rules were agreed with the project partners such as WE (Würth Elektronik) to enable a later process transfer. Additionally, expected placement accuracies and associated required IO pad, capture pad and interconnect dimensions were defined so that a proper connectivity between the several components of the flex/stretchable subsystem can be securely ensured.

First, a test vehicle was designed, using only dummy chips, for the purpose of fabrication feasibility and testing of single processes and reliability. After that, a second prototype was designed from the lessons-learned of this test vehicle, to process functional devices towards a functional flexible prototype.

For the functional prototype, a major change was implemented within the project: the processor chip being finally only available in form of few devices in multi-project wafer (wafer level thinning of devices not possible and high residual stresses in single devices), and the RAM memory chip not withstanding high temperature (required a.o. for polymer curing in thin flex embedding) it was decided to mount the active devices on the top surface of high-density flex instead embedding them inside it.

The requirements were synthesized with UC contributors in the EU Deliverable D2.4: Requirements and specifications for UC4: Cardiac Monitoring Patch.

WP3 Design, Modelling & Simulation

Task 3.2 UC2 design (Low cost thermal imaging systems)

Work has been mainly focused on the design definition jointly with structuring process flows to be performed at FhG IZM (Figure 6). GDSII file of the ROIC chip (CMOS read out IC) and 17µm pitch MBA (Microbolometer Array, thin MEMS membrane, forming the pixels of the imaging systems) has been finalized and has been provided by IDEAS (chip layout with wafer shoot map) in Januar 2020 for first design drafts and alignments.

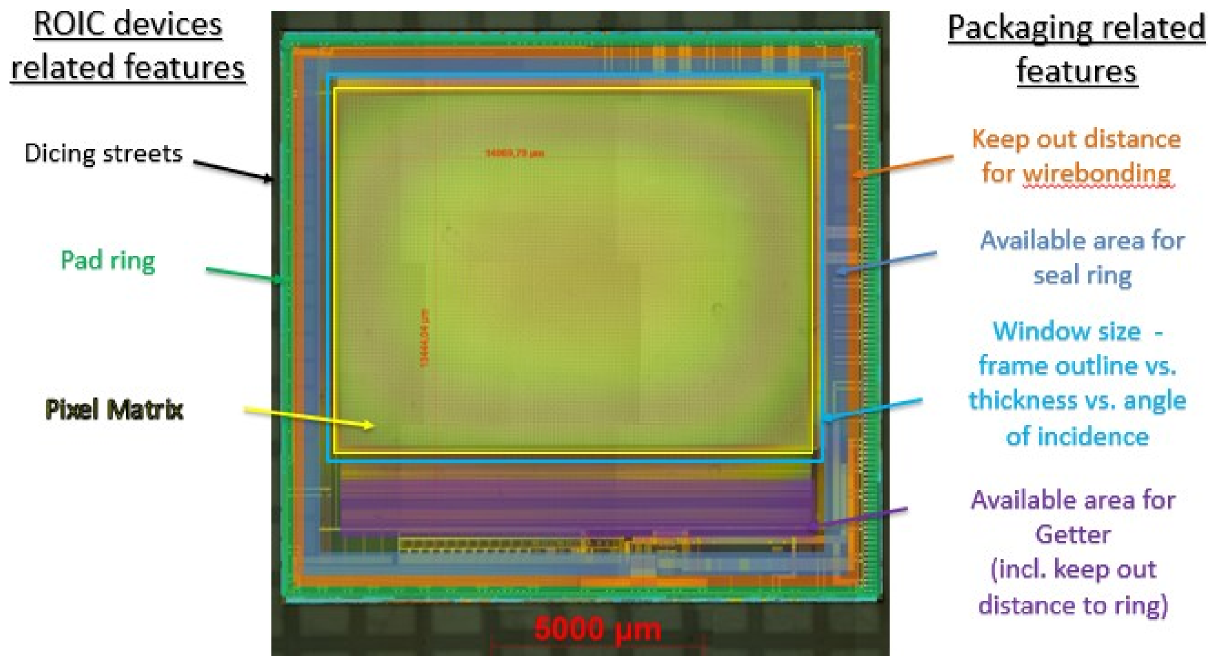


Figure 6: Example of IDEAS ROIC chip with packaging related features

Design of the ROIC/bolometer 200mm wafer layout has been reconstructed based on the ASIC shot map of the ROIC/bolometer chip and the single chip GDS (last metal layer and top passivation opening). Wafer layout were controlled and verified by comparing to a probe card wafer delivered in Mai20, which permit to fix the wafer layout grid and to circumvent any possible physical mismatch by 9’ mask designing for WLP.

WLP features have been implemented based on D2.2 boundaries, for example for the sealing bond rings depending on ROIC/bolometer top passivation thickness vs. bondring line crossing of top metal layer of ROIC as well as correspondingly to the considered cap topology/ies.

The wafer layout was iteratively improved and finalized, regarding design for Wafer Level Packaging (co-design NNFC/IDEAS & IMS bolometer platforms). Efforts were concentrated on extensive co-design to avoid later double processing work for each of sensor wafer types, ie. IDEAS/NNFC and IMS/XFAB. All of the IZM wafer joint layout has been finished in considerations of both the NNFC & IMS layouts of the bolometer/sensor devices.

In general, following works were performed:

- 200mm GDS full Wafer Layout reconstruction vs. Real wafer – Wafer layout verified (pitch, dicing streets, vs. Chip clustering/shot map on wafer) based on Dummy ROIC wafer (last metal layer & top pass open) delivered by IDEAS (Figure 7)
- GDS Chip Layout: implementation of corresponding process features
- Finalisation WLP Wafer layout vs. Process flows vs. Topologies (monolithic cap etc…) + design freeze.
- Seal ring position: Alignment with IDEAS and IMS for NNFC and XFAB MBA design
- Wafer Lithography and bonding marks sequence
- Getter: marks ok, implementation cross-checked with European industrial Provider
- wafer alignment: (aim: keep the design in all process flows compatible)
- Alignment IDEAS/IMS/IZM for XFAB design (Base/Probe wafer with Al for Pirani MEMS @ IMS)

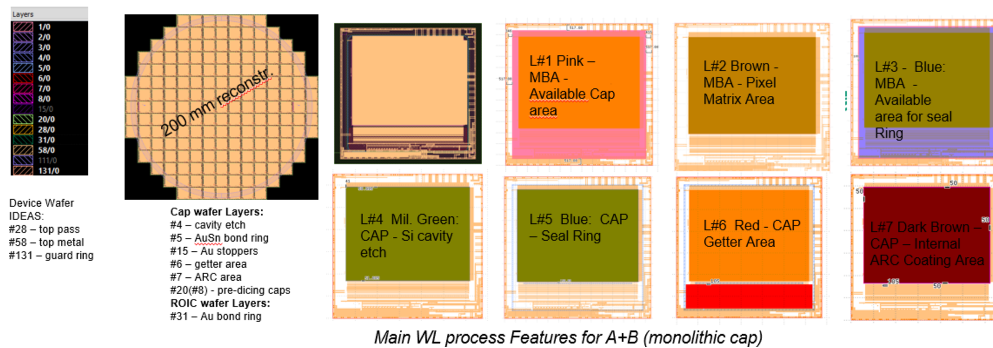


Figure 7: Wafer pre-layout and WLP features

The final wafer layout for WLP is only briefly shown in Figure 8, the entire layout enclosing more than 30 layers. Since the Pirani wafer are conceived on the IDEAS base layout, the WLP layout is compatible for two separate tracks:

a. WLP of wafer from IDEAS (Norway, MEMS made in South Korea @ NNFC),
b. WLP of MicroPirani from Fraunhofer iMS in collaboration with USN (Norway).

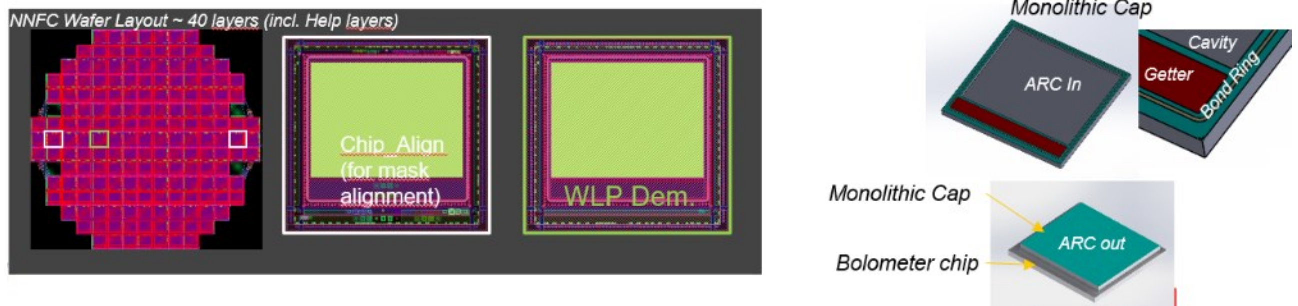


Figure 8: final layout overview for wafer level hermetical capping of bolometer

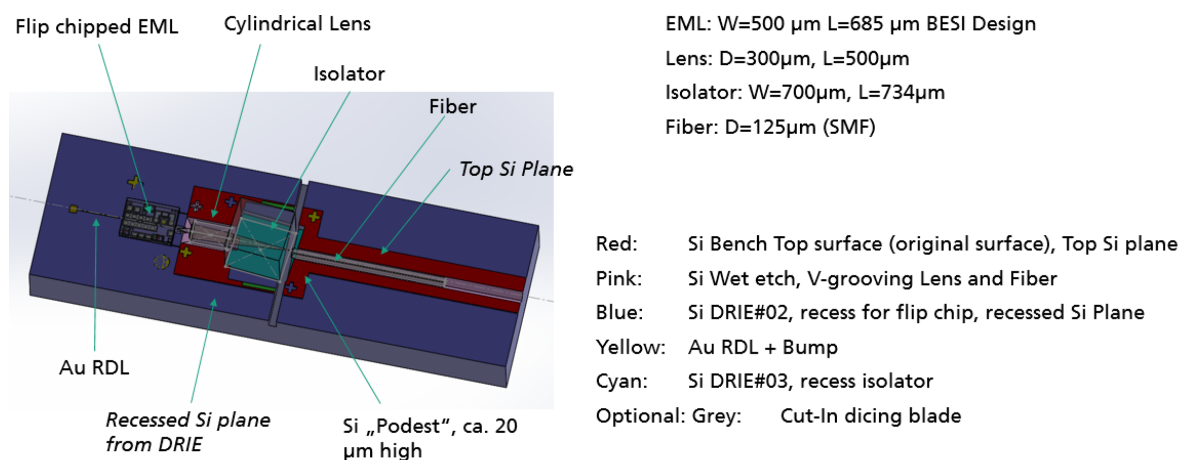
Task 3.3 UC3 design (Passive fibre alignment for single mode transceivers)

In the task, following layouting works have been done and can be summarized as follows:

- Design of Si-Bench for 3D passive alignment
- with V-Groove for alignment of optical elements (lens, fibre), defining the optical axis
- Si-Microstructuring of 3D-stoppers for passive alignment of EML chip (Electro-absorption Modulated Laser), 200 mm wafer platform
    - Reticle Layout AuSn self-alignment: Done (for WP4 P&P and AuSn Solder reflow with solder sustained self-alignement of EML to the mechanical vertical z-stoppers and lateral X & Y-stoppers)
    - Reticle Layout precise Au Thermocompression: done (for WP4 Au Thermocompression Bonding with precise flip chip bonder
- Design of HF-RDL done (based on HFSS / High Frequency structure simulator)
- Design for Bumping with Au and AuSn micro-bumps
- Si bench for machine testing for BESI for thermocompression bonding

Using 3D-CAD (Figure 9), dimensioning and relative positioning of the different elements/features like the X/Y lateral mechanical stoppers, Z-Spacers (vertical mechanical stoppers), v-grooves, wet etch cavities, have been drawn for 3D representation of the bench taking also into account the beam travel simulated by DPH. Based on those 3D-CAD drawing, the layout for wafer processing have been then extracted.

Based on the overall Silicon bench concept, intermediate test vehicles were also integrated into the wafer reticles with the UC3 silicon Bench for significant testing of the assembly technologies (Flip chip laser with “fiber groove only”, i.e. no lens, no isolator). For both assembly technologies, those aim for different purposes, amongst others flip chip assembly basic tests, fiducial recognitions, simplified optical test after EML bonding for verification of correct final placement of the EML relative to the optical axis as well as metallographic cross-sectioning.



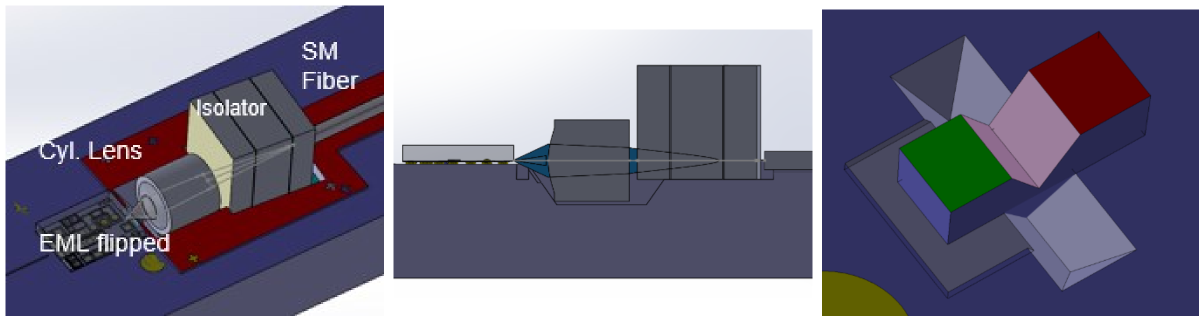


Figure 9: 3D-CAD Si bench, concept, elements, X/Y stopper for self-alignment

Figure 10 gives an insight on the pre-layouting of silicon bench, with the relative places of the optical elements, the features to be etched and the HF-lines to be fabricated onto the silicon bench for driving the modulator embedded onto the EML device after its flip chip assembly. Different variations were gathered, for example using a single lens array or isolator, instead of 4 single elements, however due to the 1.6 mm pitch of single TX-Units it was not compatible.

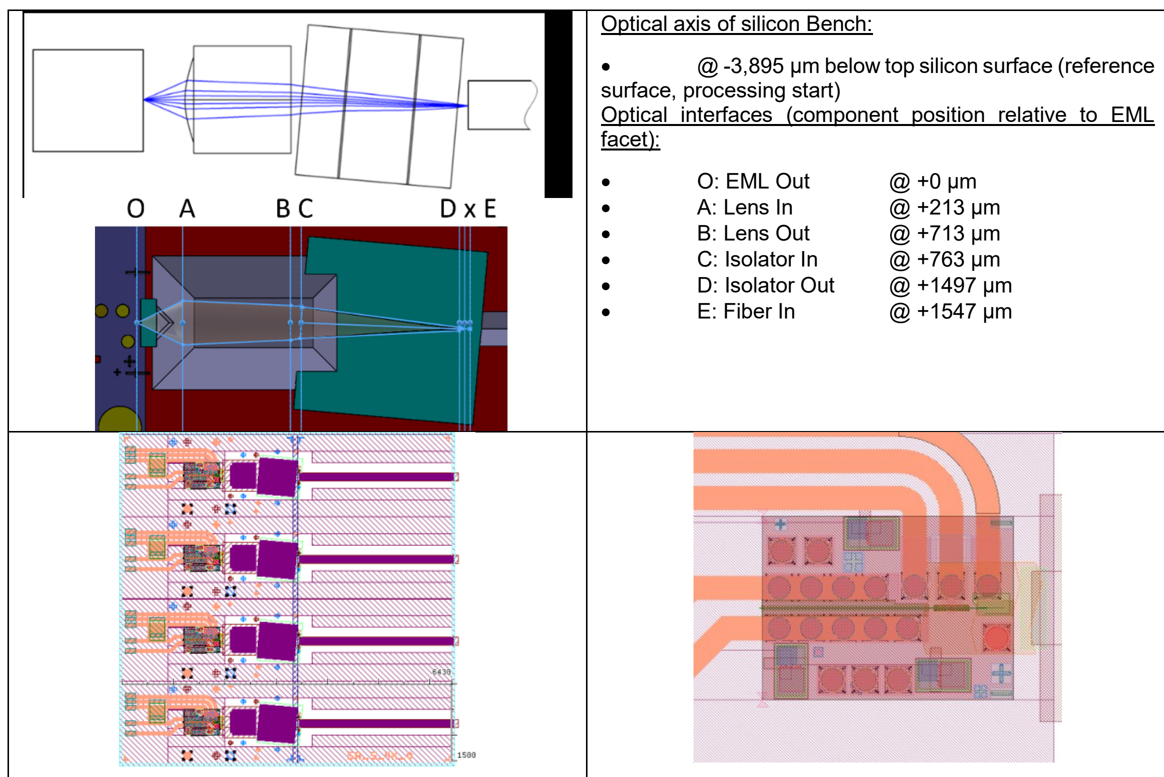


Figure 10: Pre-layout GDS of 4x Channel Silicon Bench for Assembly of single EML (solder self-Alignment, gold thermocompression @ IZM) and left, "TCB" (Thermocompression Bonding @ BESI) and respective view on EML and HF routing, left solder self-alignment with stoppers, right, TCB (HF-routing to be still implemented)

In order to implement variation a base reticle was created, whereon features then were varied to implement sub-variations for packaging (bump quantity, bump diameter, stopper size etc)

The base reticle comprises layouts of different complexity for both chip variant (straight and tilted) arranged in diverse simplified test vehicles embedding:

1. only the laser and bumps for control of shear testing,
2. simple layouts with also 3D stoppers to test the 3D-Assembly,

3. with HF-RDL and fiber grooves to test the passive alignment and perform simplified reliability tests (for example thermo-cycling)
4. and the entire optical bench including all elements in the scope the final demonstration:
    - for the assembly technologies at Fraunhofer IZM
    - for testing the pick-and-place machine of BESI Austria

Since the processes involved for the fabrication of the silicon bench are for all the same, apart from bumping, which take place at the end of the fabrication, all the substrate designs for both flip-chip assembly technologies and both EML chips were merge in a single common 200mm wafer layout and reparted in the 4 wafer quarters (Figure 11). This permits a more efficient approach:

- by limiting the number of masks required for processing,
- With an increase of the number of wafers in the process batch and so a increase of test wafers available for WP4 setups
- and consequently limit the risk on processing and adjust in consequence the most promising designs,

instead of having multiple different runs in parallel, with complex lithography works and possible process overload/bottlenecking.

In order to also test the lithography capabilities and the achievable results, an additional test layout has been also conceived and added in a repetitive manner over the entire wafer for the sake of control of process results on silicon microstructuring on slanted structures (created by the Si wet etching) and to get informative results to adjust the layouts of the benches accordingly if necessary.

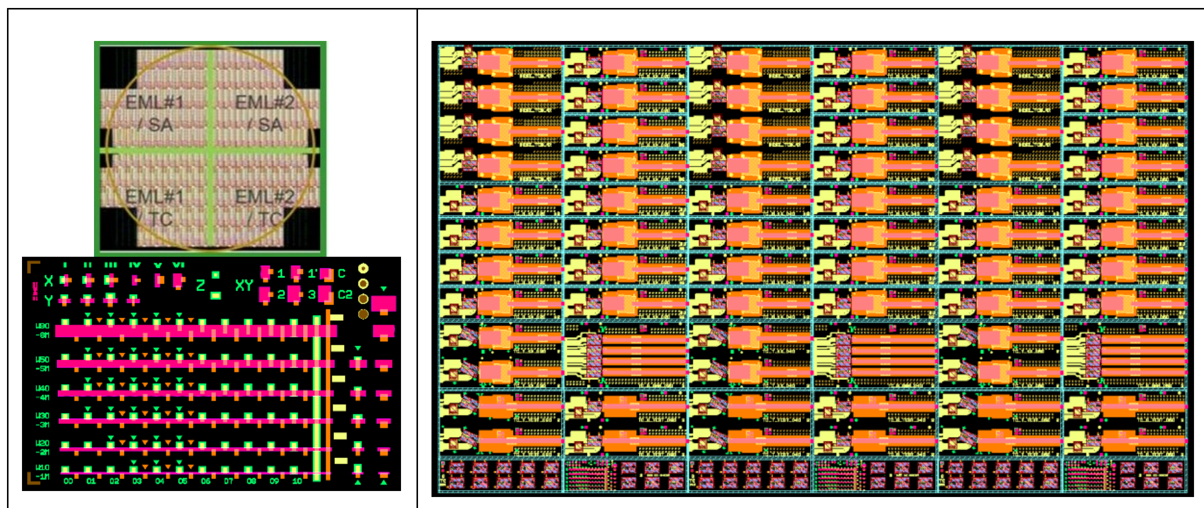


Figure 11: View on common wafer layout and its partition, the lithography test field and one of the base reticle

The major drawbacks of fusion of all the layout onto a common wafer layout are

1. The wafer complexity is getting very high
2. the quantity of wafer to be processed can become too large and take correspondingly more time for the batch to go ahead and the large increase of variations present on a same wafer.
    - 2x Assembly technology
    - 2x Laser device variant

- 3x shifted bumps for self-alignment
- 3x different bump diameter for thermocompression
- 4x base layout

The 4 base layouts of the submounts for the 2 different EML chip versions and for both flip chip technologies (Self-alignment and thermocompression) are reported in Figure 12. The submount is ca. 5.8 mm long and in a 1.6 mm pitch on the wafer layout. Dicing streets are 130 µm wide for correct mechanical dicing and clearance to 3D topography.

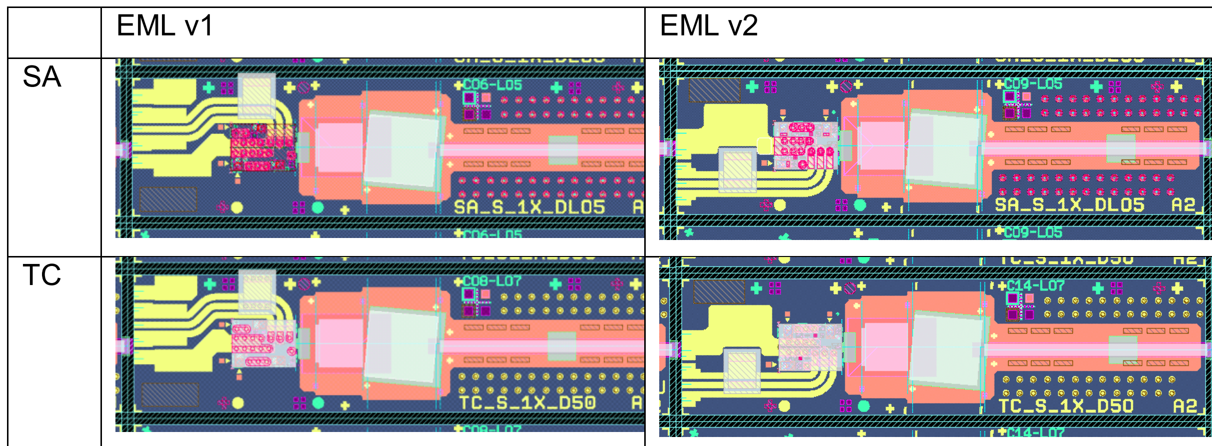


Figure 12: final base layoutd of the 3D Silicon submount, for self-alignment and Thermocompression for two chip version (v1, v2) for precise passive alignment of Flip chip laser, Lens, Isolator and fiber for building a Transmitter Submodule.

Apart from layouting, optical simulation works were also performed for Chip-to-fiber coupling in order to support / better understand the experimental results obtained (Figure 13) and in the scope of the characterization of TX-sub-module fabricated on 3D Silicon bench (Figure 14).

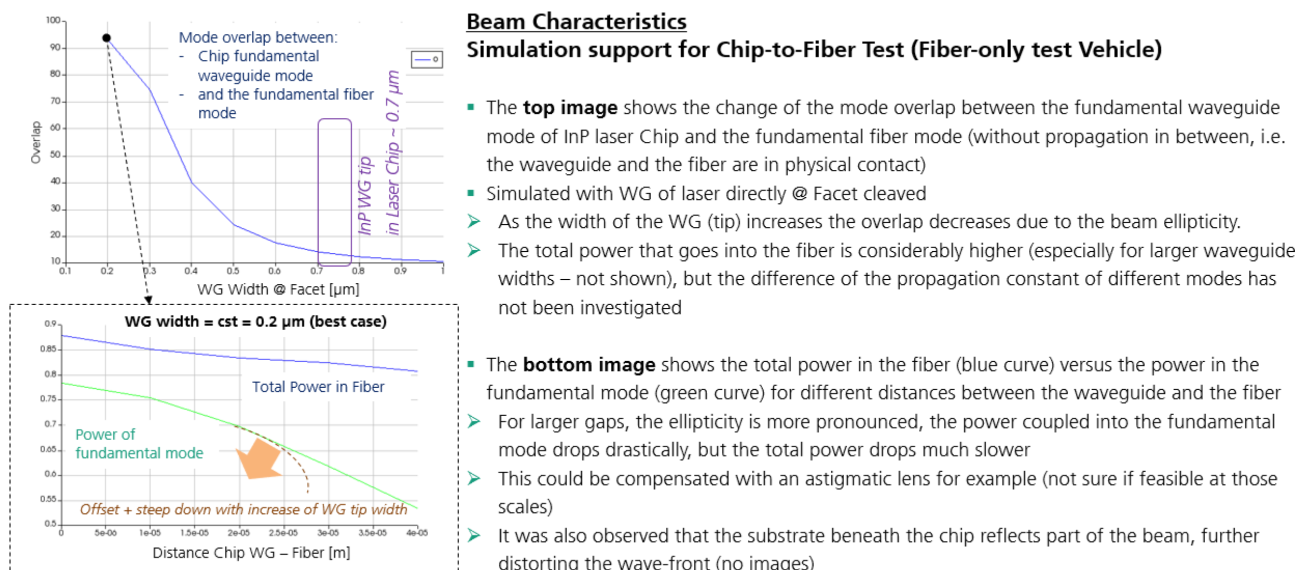
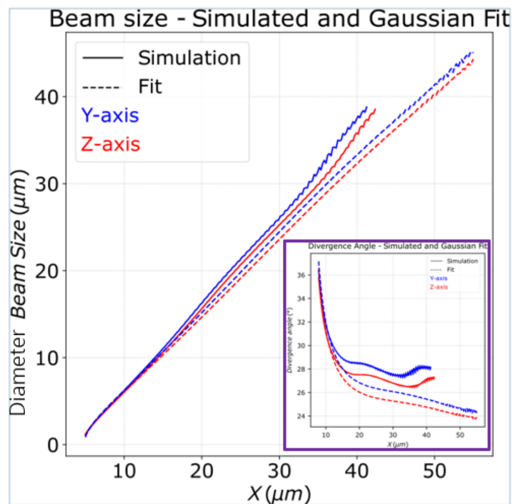
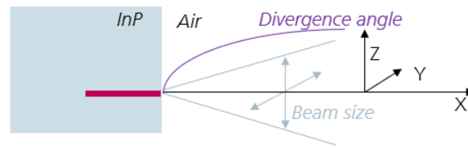


Figure 13: Simulation support for chip-to-fibre testing (understanding of experimental results)





Beam Characteristics

Spot Size – Divergence (=> Sub-module Dimensioning)

- The fundamental mode of the waveguide in the InP laser was excited and following the propagation inside the waveguide and in air was simulated
- The idea is to observe the beam propagation in free space and validate the characteristics of the lens
  - The mode field diameter (1/e^2) was found from the simulation results (Simulation) which were also fitted to a Gaussian profile (Fit)
  - The difference between the MFD on the two axis show the ellipticity of the beam
  - The divergence angle (inset) is max 30deg, so a numerical aperture of 0.5 should be fine
  - The aperture of the lens (500um) positioned 200um away from the laser facet is also large enough to capture the whole size

Figure 14: Simulation for sub-module dimensioning

This work supported the flip chip integration on the 3D Silicon Benches, and was necessary in order to better understand the opto-electrical results of intermediate test vehicles with Lasers precisely mounted by Flip Chip on the 3D Silicon substrate and lighting directly in glass fiber (purpose: verification of post bond alignment of laser to optical axis).

Task 3.4 UC4 design (Cardiac monitoring system)

a. Passive test vehicle

FhG-IZM created, improved and fixed a first passive test layout (Figure 15) for the process developments regarding high density flex fabrication with embedded ICs and flex on stretchable substrate integration. The test layout is based on IMEC-NL's MUSEIC device, which is a SoC available as non-packaged bare die. Due to non-signed NDA and lack of gds2 design data of the SoC, the die pad layout was re-established at FhG IZM based on coordinate list and given pad dimensions from IMEC-NL. Due to limited number of available functional MUSEIC devices, the test layout for thin die embedding into flex included dummy devices based on the layout of the MUSEIC.

The MUSEIC requires a flash memory for data storage. Based on that, the test layout includes dummy devices of flash-memories which had originally also to be integrated into the flex as thin device. Functional flash memory devices had to procured and could only be used later for the fabrication of the final functional demonstrators (one single wafer available). A simplified overview of the test layout with the MUSEIC and flash memory is shown in the Figure 15. It comprises amongst others fiducials for chip bonding and test structures, especially daisy chains from flex-to-dummy chip-to-flex to verify the interconnect integrity. Due to non-fixed final delivery source of the flash memory, which also need to be available as bare dies, a representative layout of a flash memory was taken out of FhG-IZM layout database to enable the start of the test layout and the fabrication. Both dummy chip layouts, MUSEIC and flash memory, were comprised on one common wafer layout to enable their simultaneous fabrication at FhG IZM.

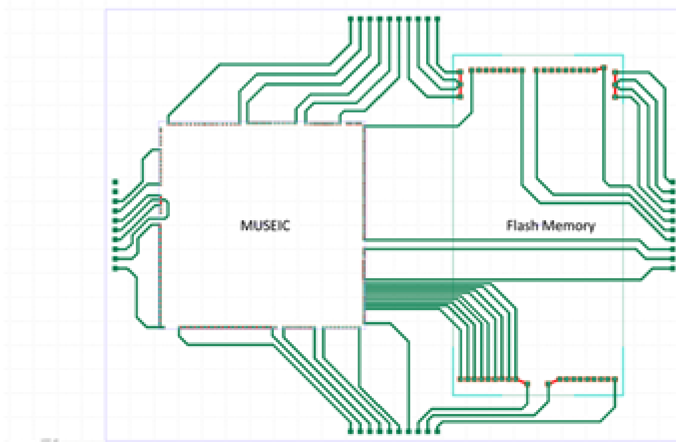


Figure 15: Base layout of the test vehicle (chip embedding in flex) with interconnections of the flash memory and MUSEIC dummies die.

After the first Die-to-Wafer trials, the design of adhesive layer was also ameliorated. Therefore, the layout was re-adjusted, in order to reduce air enclosure under thin dies after placement

The test layout allows daisy chain measurements over most of the different levels of interconnections between chips, thinfilm flex and stretchable substrate as well as partial measurements for failure location. The Figure 16 shows the wiring in TPU to the chip embedded flex.

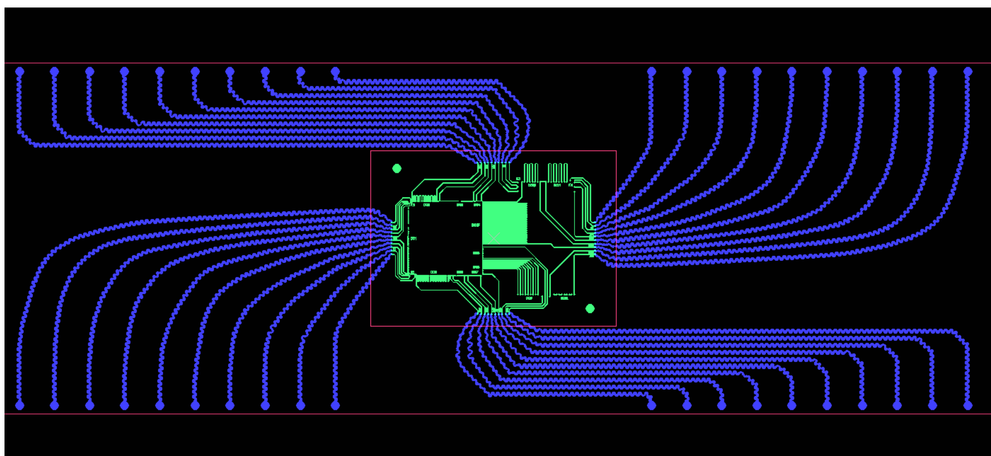


Figure 16: Base layout of the test vehicle thinfilm flex with embedded test dies embedded in stretchable patch matrix

b. Active test vehicle

Lessons learned were extracted from the 1st flex chip embedding fabrication trial to generate the final layout for functional devices for 5.4.

Fraunhofer IZM has layouted the flex for the functional demonstrator, which carries the MUSEIC the Flash Memory IC, a double LED, an infrared diode, an accelerometer, a voltage regulator, ESD protection devices as well as several passive components. Since the MUSEIC was not available as wafer and only one wafer with Flash memories was available, it was not possible (or had high risk to fail) to thin and embed the active dies, if the approach of extreme thinning and chip embedding would be used.

Based on this, the technology approach for the functional flex module was slightly changed to a solution were the chips are not extremely thinned and embedded into the flex. Instead of this, the ICs are assembled flip chip like with stud bumps, together with the other components onto the surface of the functional flex. The flex hosts the same components as the molded SiP version from IMEC-NL with Boschmann. Figure 17 shows the schematic cross view of the intended build-up of the flex. It includes two internal routing layers as well as a top and bottom pad layer. The bottom side pads is used to contact the flex SiP later with the stretchable patch.

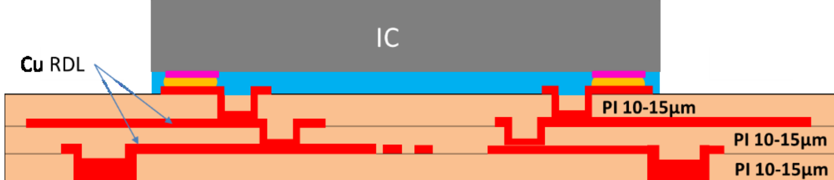


Figure 17: schematic cross view of thin film flex with IC component on top

Figure 18 shows a layout view of the flex SiP, which was reviewed and acknowledged by IMEC-NL. The SiP has a total size of 24,6 x 17,6mm2. The total expected thickness is 45-50µm.

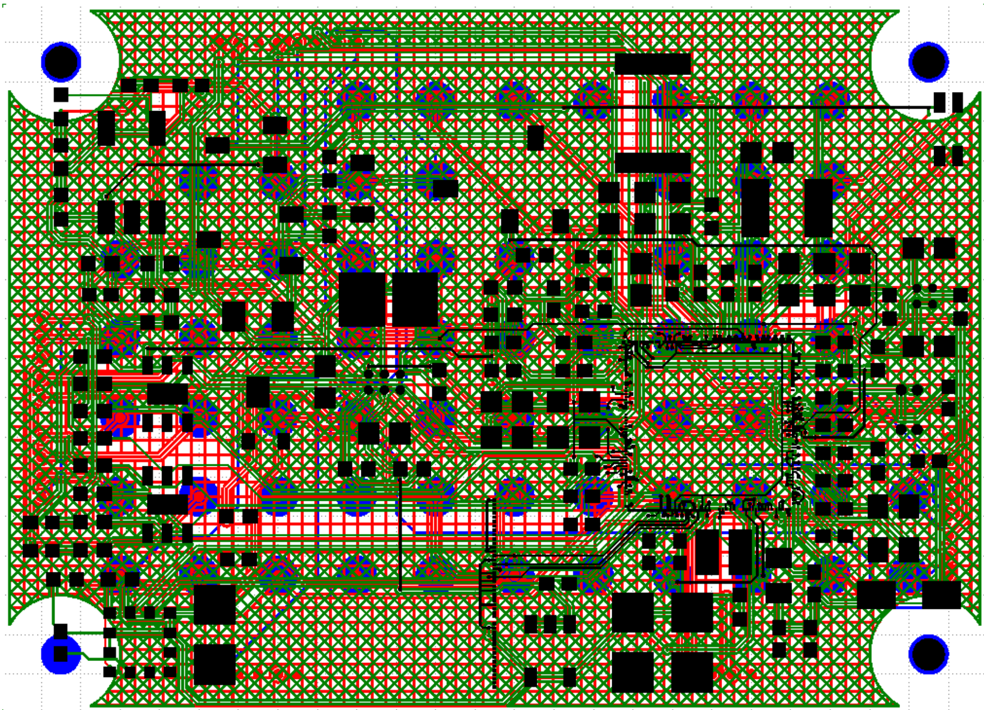


Figure 18: Layout view of functional flex SiP with four metal layers. blue=bottom side pad layer, red=first internal routing layer, green=second internal routing layer, black=top side pad layer

WP4 Equipment, Processes and Software Components

Task 4.2 High precision photonic packaging

4.2 a) Test vehicle for high precision bonding & 4.2 b) Development of a Flip-Chip process for high precision assembly

4.2.a) 3D Silicon Substrate Fabrication

The fabrication process concentrated onto a first version of the 3D Silicon Substrates (“WP4 grade”) in the scope of generating substrates valuable for performing the 3D precision flip-chip processes. Without 3D-substrates, the Flip chip processes intended in APPLAUSE (mechanical stop on vertical stoppers for flip chip thermocompression, on vertical+lateral stops for flip chip self-alignment) cannot be experimented.

After WP3 Wafer Design fix by summer 2020 and entire process flow definition, first process masks were ordered. The fabrication necessitates basically 7 masks:

1. Vernier for 100 crystal orientation, (Wet Si etch, Hard Mask)
2. V-groove etching, (Wet Si etch, Hard Mask)
3. z-stopper level, (DRIE Si etch -4 µm, Spray PR Mask)
4. Flip chip recessing (DRIE Si etch -31 µm, Spray PR Mask)
5. Isolator recessing (DRIE Si Etch > 75µm, i.e. 110 µm, Spray PR Mask)
6. Routing (gold electroplating 3 µm, Spray PR Mask)
7. Bumping (Au 24 µm, AuSn, Spray PR Mask)

The wafer layout is divided in 4 quarters dedicated to different technologies, the upper part being designed for assembly with solder driven self-alignment, the second half being for gold thermocompression. The left part is designed with the first EML chip version of ALMAE, the right part for the EML version #2.

The merge of all designs is for synergic convenience and possibly to catch up time-loss due to COVID-19 impact and limit the work spread by multiplying process runs with the complex process flow due to high topography. The merge is justified since basically the fabrication of the Si-bench for both assembly technologies differs only by the last process block (bumping). The merging in a single wafer layout of the different designs allows more robustness and flexibility regarding risk mitigation, more wafers being processed in the same batch.

A. Silicon Wet-etching

In 2020/Q3 process work has been started on Si-Bench in the frame of WP4. First wet etching process were set and done with the correct features sizes, first on 200mm monitor wafers (WP4) then onto high resistivity base wafers for WP5.

1. Wafer Orientation to <100> crystal direction
2. and wet etching of V-groove structures down to 270 µm nominal depth (for 500µm cylinder Lens) were performed.

However, it appeared the hardmask undercut by the etching process was too “pronounced” (+3µm deviation vs. target) leading to larger etched widths than expected and even to a merge of nearby delicate structures like some fine etched fiducials (not enough clearance between).

This would make the wafer unusable for WP5 in regards of the envisioned submicronic alignment, with a shift in Z of the fiber as well a shift in X and Y of the contact points as designed, leading to imperfectly aligned optical parts.

Therefore, most of the relevant features of differing sizes (V-groove of Fiber, V-groove for lens, V-grooves for stoppers, test v-grooves) were manually measured for highest precision on two wafers before and after hardmask removal in North, South, West, East, Center to verify the undercut homogeneity on large (lens, fiber grooves) and small (stoppers) etched structures.

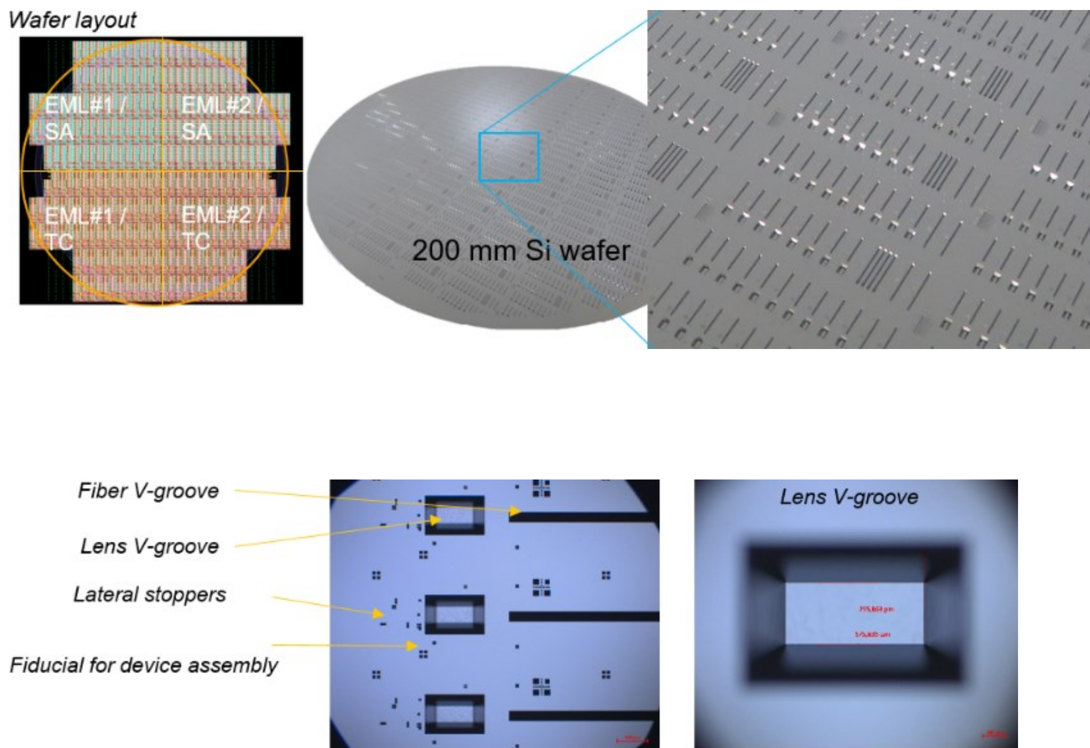
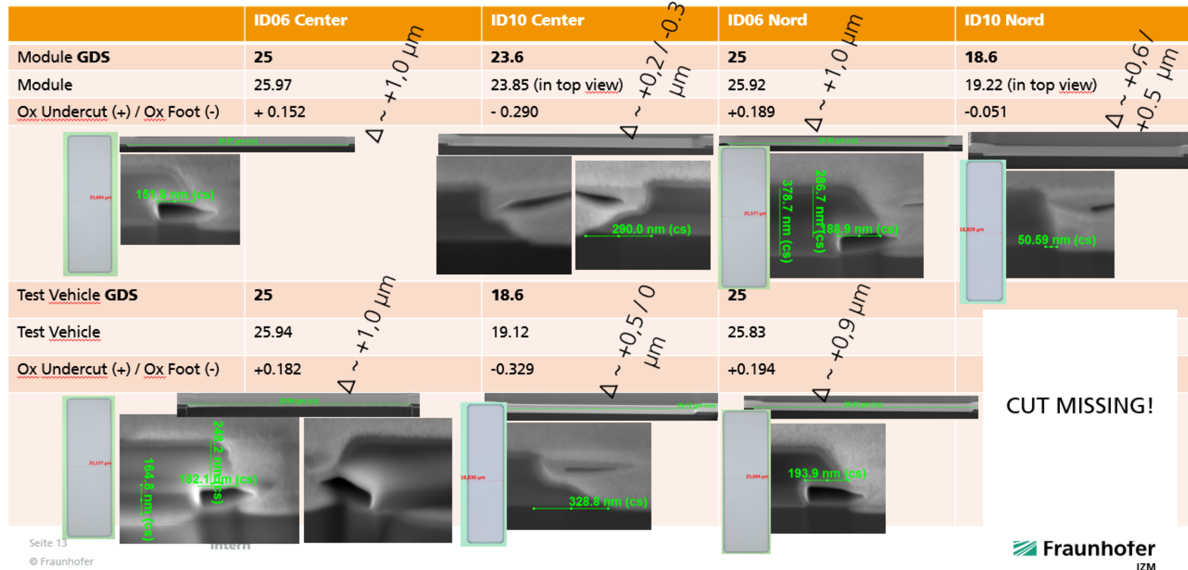


Figure 19: Synergic wafer layout compiling 2 flip-chip assembly technologies (SA- AuSn Solder Self-alignment; TC: Au Thermocompression) for 2 laser device versions. Silicon photonic bench after deep wet etching of the 200mm Silicon wafer

Based on this, a corrected/compensated layout was generated. Since all wafer were scrapped, a new wafer batch had to be restarted from beginning, also with high resistivity silicon (expectation of higher HF performances of the bulk material), to improve the feature size below 1µm deviation, as a “WP5-Grade” version of the 3D-silicon bench (*Figure 20*). The relaunch included also the identification of the correct (100) crystal orientation using wet etching of precise nonius features.

The new mask performed very well on monitor wafers by end of 2020, all structures deviating only by ~0.2 to 0.5 µm to the desired values. This process was transposed to the WP5 wafers for final demonstration.

Using an automated inspection tool (limit of tool resolution ~ 1 µm due to pixel/digitalisation), a precision under 3 µm in width (1.5 µm one side) over the 200 mm wafer area and under 1µm (0.5 µm one side) in 150mm wafer core could be reached for this high resistivity wafers (T5.3.2), assessed by manual cross-control with light microscopy measurements.



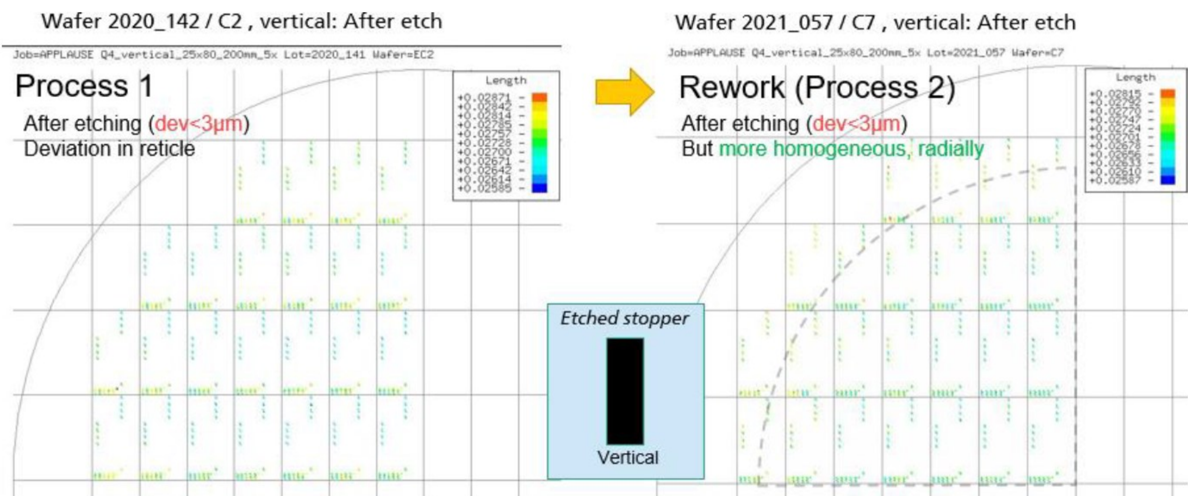
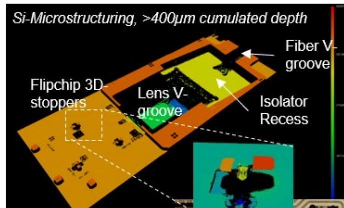


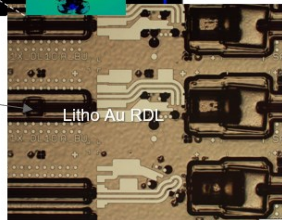
Figure 20: Hard mask process evaluation (top), resulting in improvement of feature size deviation <1 µm in 150mm wafer core of the 200 mm Si bench wafer (bottom).

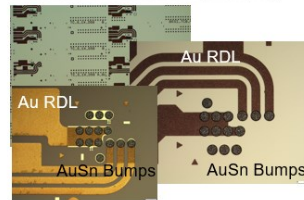
B. silicon dry etching

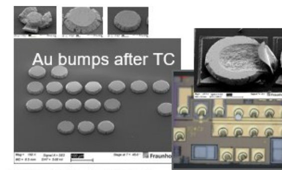
Next steps was first the setting-up of the dry-etch microstructuring (micromachining) of the silicon using lithography and intensive deep DRIE processes (3x, one after another with different target depths) on already challenging high topography wafers (due to deep v-grooving). Processes were individually tested and combined in a fabrication flow. Metallisation tests (RDL, Bumping) were also tested in parallel, first on planar wafers, for rough setups/short loops (Figure 21).

The shortloop bumping materials were further exploited to verify the bump compression with 3 different bump diameters (D20, D40, D50), to characterize the HF routing and generate first flip chip assembled InP laser onto the HF routing, inclusive 50 ohm decoupling resistor (@ March 22), and provided for characterization (Figure 29). This aimed to perform basic DC and HF characterization of the InP laser after flip chip.









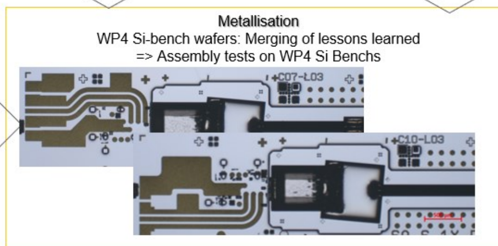


Figure 21: Si deep etching/full microstructuring, metallization tests (routing bumping) and combination of boths

- Done: Si Deep Microstructuring (Figure 22), with all structures needed (Figure 23), basically
    - Z-stop level
    - Recess of flip chip area, with formation of stoppers
    - Light path Open and recess for isolator
- Done: Metallization of 3D-structured silicon bench (Figure 24)
    - Thick gold of 3 µm, for the signal lines, High-frequency

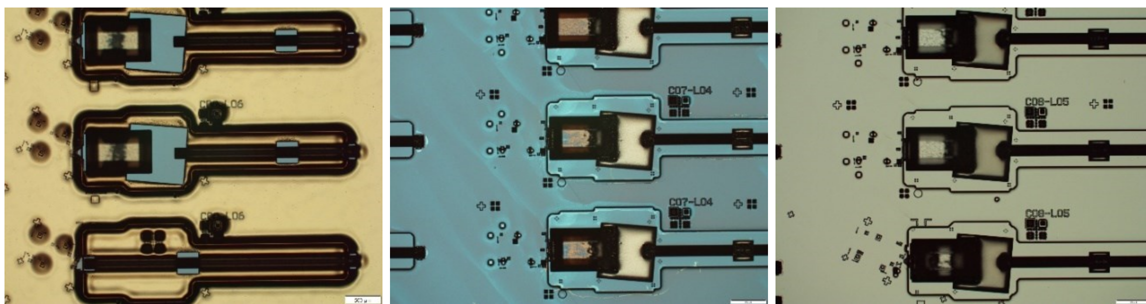


Figure 22: WP4 Silicon Bench, recess of isolator and light path open: lithography on high silicon topography (left), after dry silicon etching (center) and surface desoxidation (right)

The resulting 3D structure is illustrated in Figure 23 with the CAD schematic of principle of the targeted SiBench. By means of light profilometry it is basically possible to inspect the resulting highly complex structure.

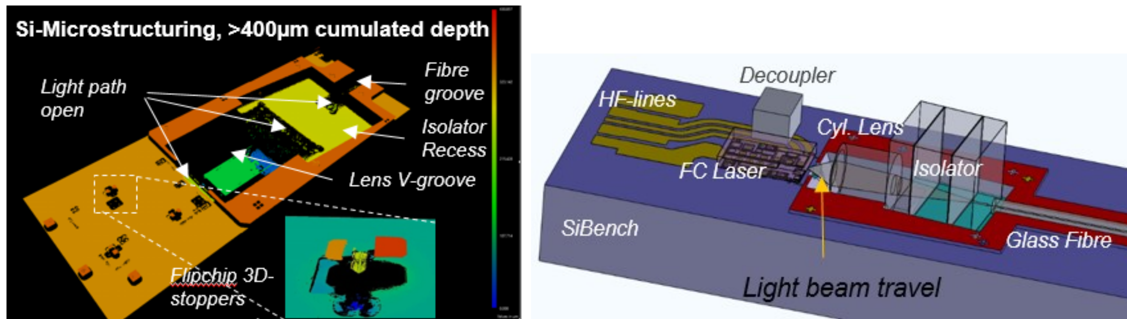


Figure 23: 3D light profilometry measurement after Silicon structuring (Left) and CAD of targeted Bench (right)

C. 3D Silicon Substrate Metallisation (Au RDL, Bumping)

The next major task was the metallisation of deeply-micromachined Silicon wafers for routing. A thick electroplated gold was retained, to be compatible with III-V lasers (avoiding any possible Cu poisoning), for HF transmission and to offer enough section (i.e. thickness) for power feed, in comparison to thinner AlSi. The routing was executed by semi-additive process using electroplating of 3 µm thick gold HF-RDL (nota: for power feed, 6µm was by UC owner envisioned but jeopardizing the overall topography tolerances) before moving towards final bumping for both passive alignment bonding scheme:

- Gold bumps for flip chip thermocompression, by means of a high precision bonder (vision-system assisted x/y positioning) for gold thermocompression with z-defined mechanical stoppers on
- and Gold-tin Bumping for flip chip self-alignment, by combining “unprecise” pick-and-place and solder driven self-alignment as well as

The RDL metallization process could be successfully transferred on the 3D silicon bench wafers of WP4 grade (process developments) as illustrated in Figure 24 / left.

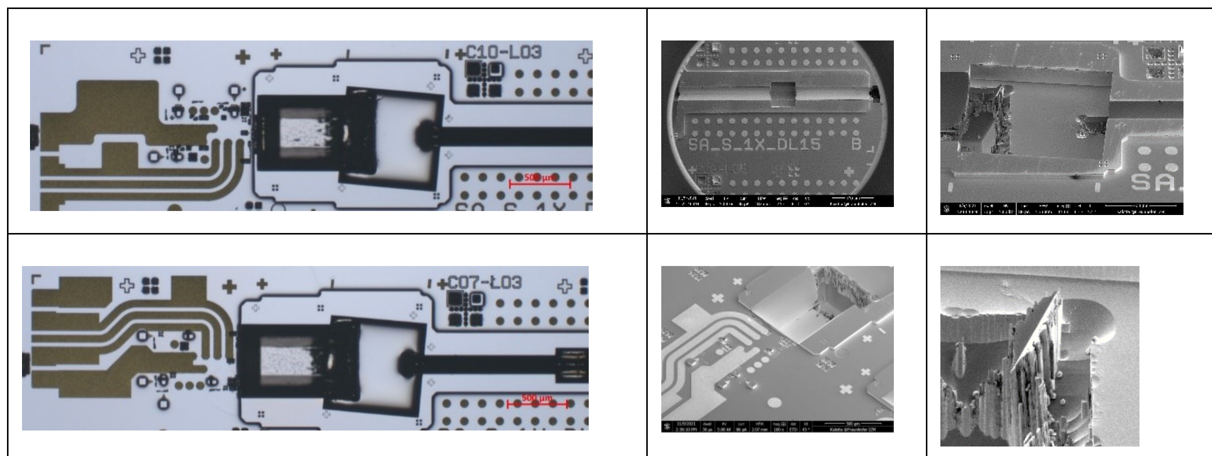


Figure 24: Left: Overview pictures (light microscopy) of Silicon bench after thick Au RDL metallization (for EML version 1 and version 2 of ALMAE), center: SEM views of fiber groove with glue recess (top) and lens groove with RDL (bottom); right: SEM views of 5° tilted isolator recess (top) and magnification on silicon spiking (bottom)

Figure 25 and
Figure 26 give further insight on the fabricated 3D-Si Benchs.

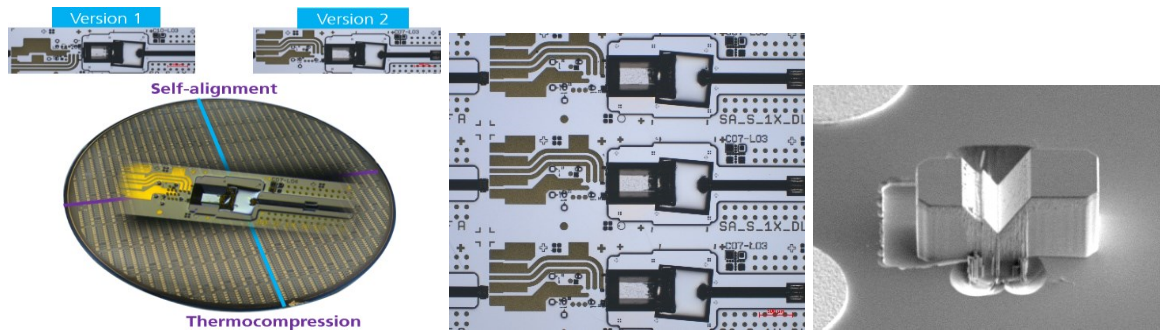


Figure 25: for Fabrication status of 3D Si Bench, 8' Wafer, with example of a 3D-Stopper (here for flip chip self-alignment in vertical position on flat and lateral position on slanted wall)

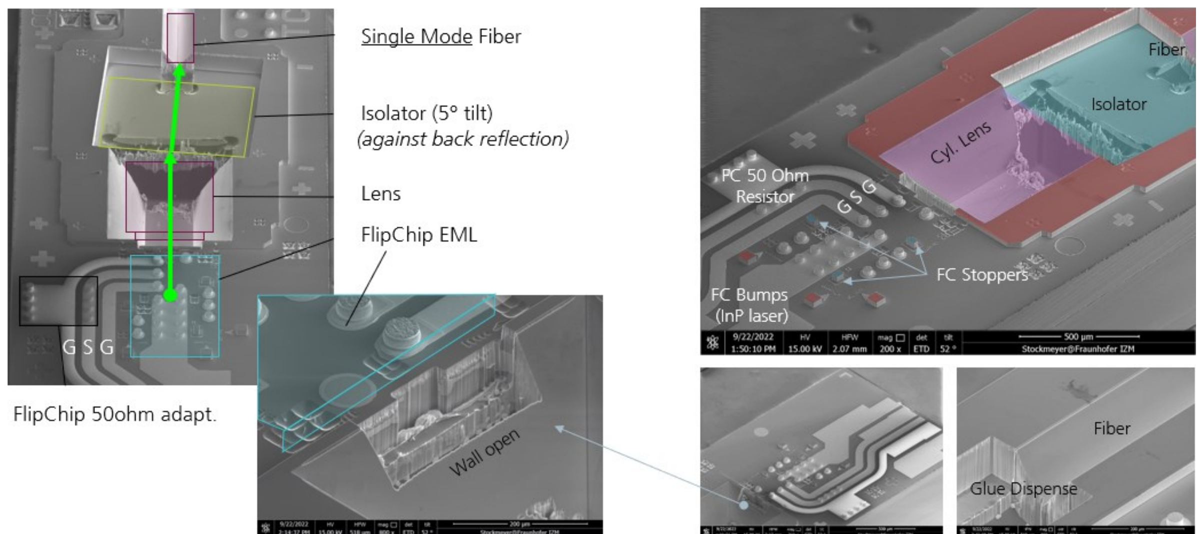


Figure 26: SEM views of 3D silicon bench with Au bumps

Despite technical issues between Silicon Structuring and metallization, with Si Spikes in Isolator recess pointing out of the photoresist and being then electroplated, thus leading to additional delays (apart from COVID-19 Frame), a first generation of 3D SiBench could be fully completed End March 2022, at least acceptable or even in the target in regards of the Au bumping height:

- for thermocompression flip chip experiments at FhG-IZM
- and process developments for optic assembly at BESI-AT (due to withdrawal of DPH, originally in charge of optic assembly and testing).

Dedicated substrates were also delivered to BESI-AT within this 1st generation, substrates having been specifically designed for their bonding equipment developed in APPLAUSE and additionally integrated in the wafer layout.

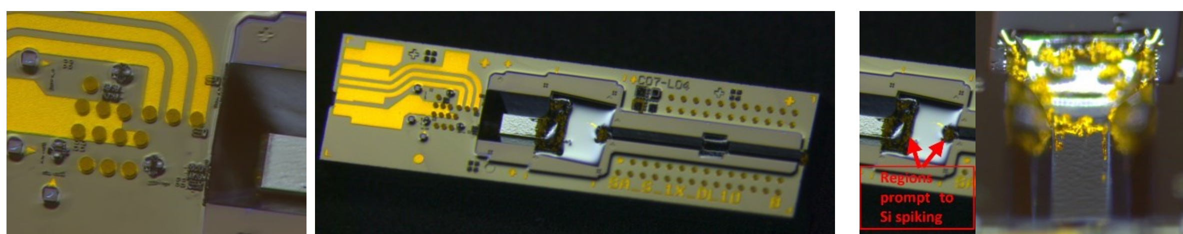


Figure 27: example of a fabricated 3D Si Submount after wafer level processing (Nota: design Self-alignment, no bumps for 50 ohm resistor included, studbumps are here additionally used).

4.2.b) Development of a Flip-Chip process for high precision assembly

A. FC Thermocompression (TC)

Using short loop wafer (ie. without stoppers), the mechanical behaviour of the Au bumps has been first studied in order to correctly size the bump needed for the thermocompression process in the forefront of the fabrication of the 3D Si Submounts. Following points were investigated:

- Au bump deformation behaviour and bump shaping/dimensioning vs stoppers (Figure 28)
- Shear tests, regarding flip chip robustness (see also Figure 119)

When bumps are directly used “as plated”, they tend to flake with shell detachment, leading to a risk of electrical shorts between two adjacent bumps. Adding a pre-treatment of the bumps prior flip chip bonding permits to resolve this issue. The buckling and barrelling remain limited even by high deformation. The effect of the pre-treatment is a displacement of the maximal deformation by around -2 to -5%, the bump being less deformed. A diminution of the bond pressure from 250 to 150 MPa reduces the maximal deformation by 10% , as well as a diminution of the bond temperature.

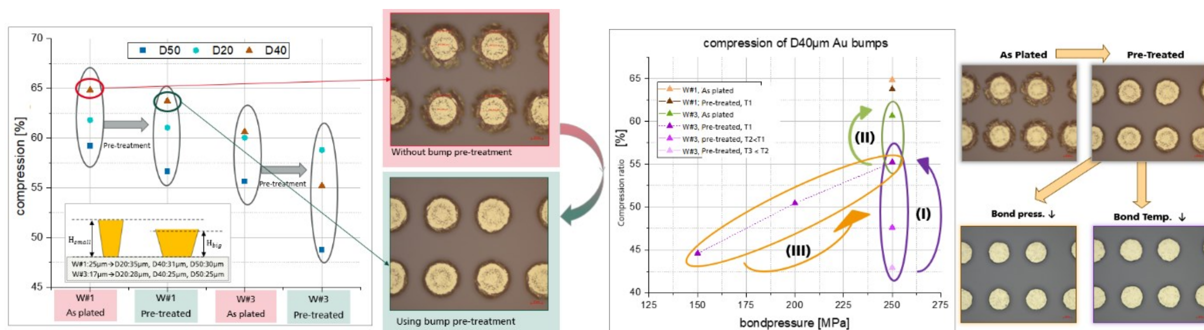


Figure 28: Testing of thermocompression behaviour of electroplated gold bumps in different diameter and height combinations (D/H - D20/H35 & 28 µm, D40/H31 & 25µm and D50/H30 & 25µm)

On short loop parts made of standart Silicon (resistivity ~ 50 ohm.cm), the thermocompression, the HF behaviour and the laser were tested (Figure 29). HF behaviour of the gold lines with standard silicon as base material and 100 nm thermal oxide is in the range of simulated values.

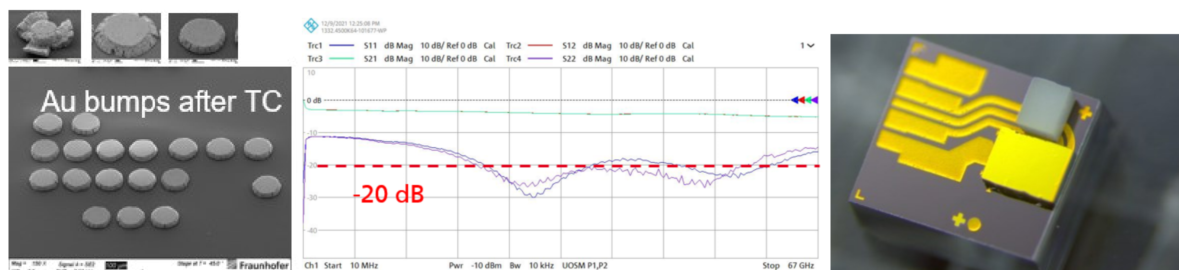


Figure 29: Evaluation of bump thermocompression and HF routing ; shortloop flip chip samples for FC characterisation

Then, as soon as 3D Si Benchs were available, first FC TC (Flip chip Thermocompression) experiments were started with a precision flip chip bonder on shortloop bumping wafers to evaluate the compression of the bumps with vertical stoppers, as reported in D4.2. Afterward, the process was transferred onto the high precision flip chip bonder, in order to possi-

bly target to the final requirement of submicrometric lateral postbond position. Diverse inspections were performed to check the integrity of the assembled parts, amongst other cross-sectioning (Figure 30).

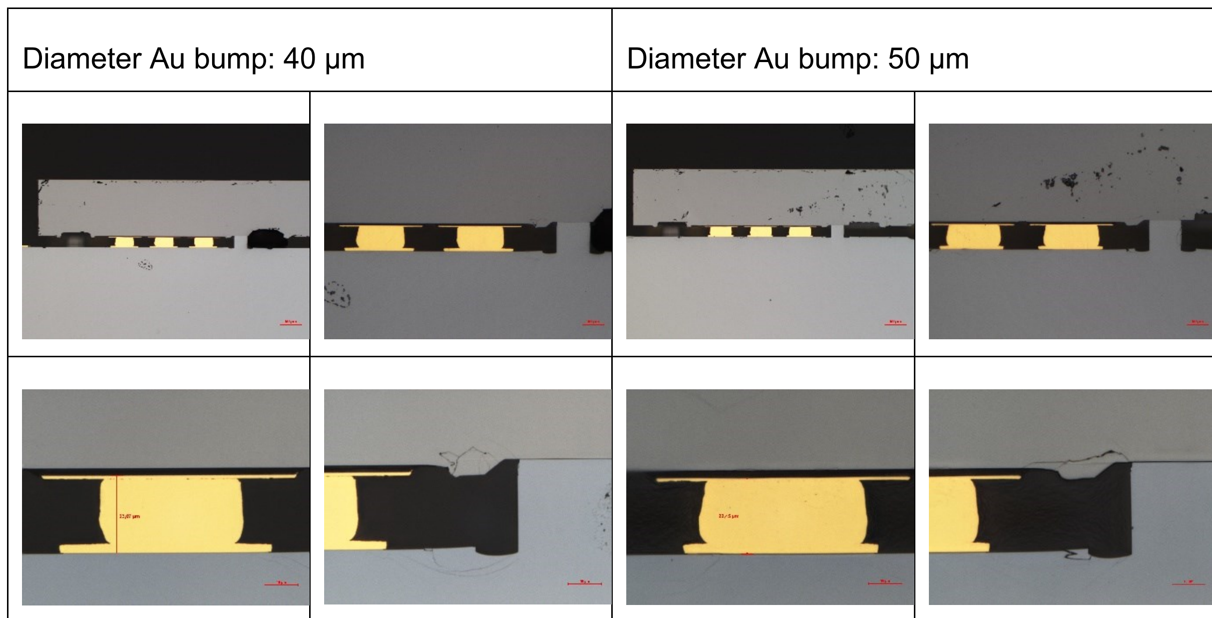


Figure 30: Thermocompression test with EML v1 to z-stop with gold bumps of 40 µm Diameter (left) and 50 µm diameter (right) (nota: cracks are preparation artefact of grinding & polishing)

The cross-sections were further inspected by SEM to examine the bond interface of the gold bump and also the z-stopper (Figure 31). The bump/chip pad interface is still recognizable but the gold bumps seem well bonded in the bump centre.

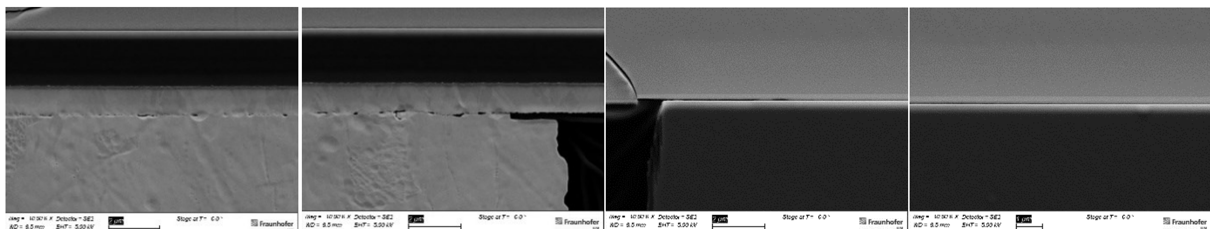


Figure 31: SEM inspection of the bonded interface at the D50 bump (left) and the vertical stop (right) after flip chip Au thermocompression process (crack in fragile InP probably from grind preparation of cross section)

In regards of inspecting the postbond accuracy, since the EML backside is metallized, the assembly cannot be examined using IR microscopy from the chip side, however through the backside of the silicon (backside of silicon wafer polished for this purpose). But, due to the gold RDL, the entire chip cannot be seen through the submount. For example, Figure 32 / Top-left, one of the z-Stop at corner does depict fracture however related in this particular case to a particle already present prior bonding (red circle on second picture), dirt most probably from InP cleaving, the Chip cleave goes to close to the z-recess and produces particles.

The postbond accuracy can be roughly evaluated by means of the markers present on the chip and submount created in the structuring of the photonic layers (do not work, the markers are not transparent (smooth) enough to see through) as well as by means of the markers and the InP waveguide (Figure 32). The EML seems laterally well aligned with the submount.

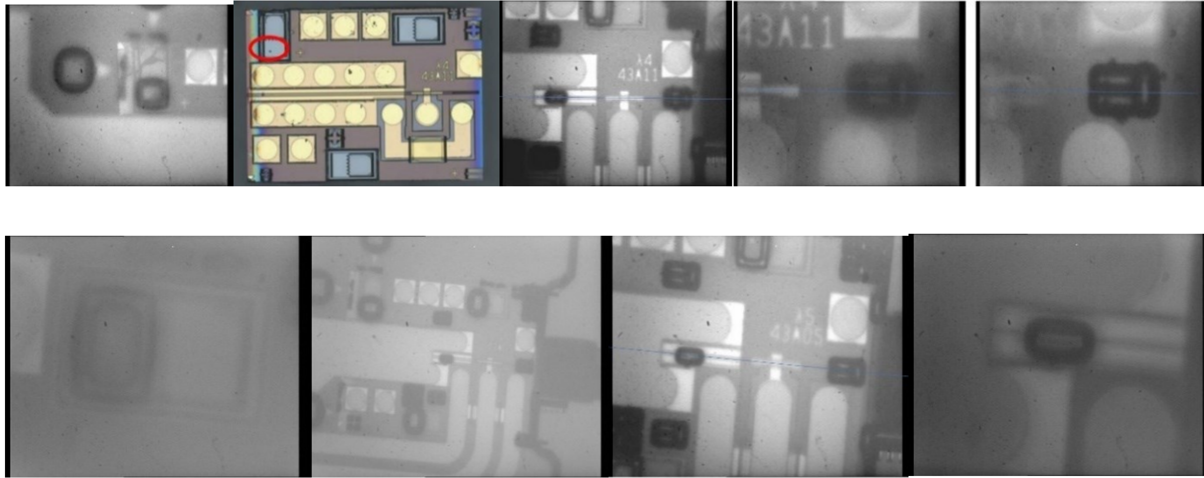


Figure 32: Infrared Post bond inspection through silicon submount "fiber only", top: example with broken InP at one of the three z-stops (sample C07-L08-D40), bottom: example without detected damages (sample C05-L07-D50)

The test vehicles were optically tested by turning on the EML and capturing the light with a cleaved single mode fiber (SMF) placed in the v-groove and approached next to the EML facet. A signal could be detected, coupled into the fiber and a typical LIV curve of the EML measured (Figure 33). On the sample with InP fracture near the z-stoppers, it is not clear, if the unusual LIV curve is caused by the chip as delivered or by the defect observed at the z-stop (Figure 31).

- ⇨ Nevertheless, this test-vehicle and associated measurement validate the 3D passive alignment.

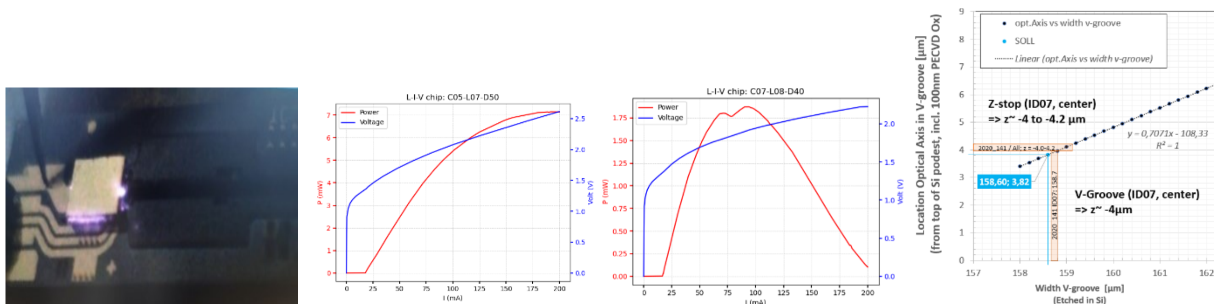


Figure 33: Tests of "Fiber-only" test vehicles with cleaved SM fiber, EML v1.

B. Solder Assisted FC Self-Alignment (SA)

First 3D Silicon Benches for FC self-alignment were also fully processed, however the Si-Spike issue led to uncontrollable AuSn bumping process. Consequently, the bumping height, composition and morphology was not compatible with self-alignment due to local bump height variation with FC unconnected bumps and misaligned laser (as reported in D4.2).

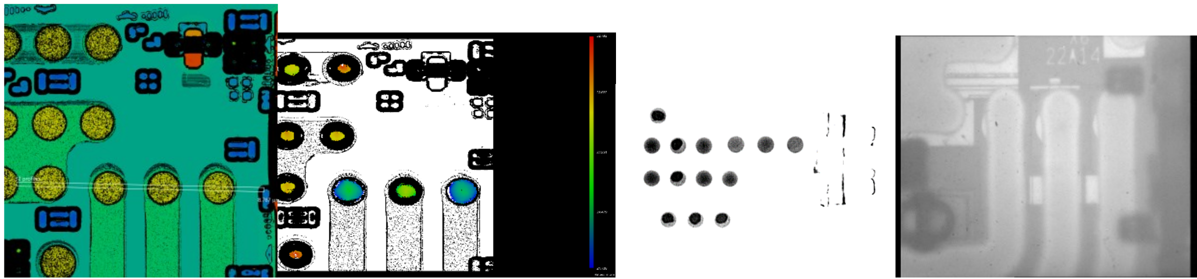


Figure 34: Comparison of Bump height inspection, as plated (left) and as reflowed (same, filtered to upper part), X-Ray and Backside Infrared inspection after SA flip chip

Several bumping rounds on 3D SiBench wafers were necessary and performed to cope with this aspect, leading to further postponements. A final 3D Si wafer could be finalised Mid-August 2022 and provided for first tentative of FC Self-alignment.

Several iterations of FC Self-alignment were performed on parts of the wafer, with some positive results as revealed by cross-sectioning onto 3D stoppers (Figure 35). Further experiments should be performed, with wafers of second generation, out of the project timeframe due to accumulation of technical issues, resource overload and overall delays (partly, COVID-19 causes and consequences).

The EU Report/Deliverable D4.2 – High precision photonic packaging - gives further insight on the work performed.

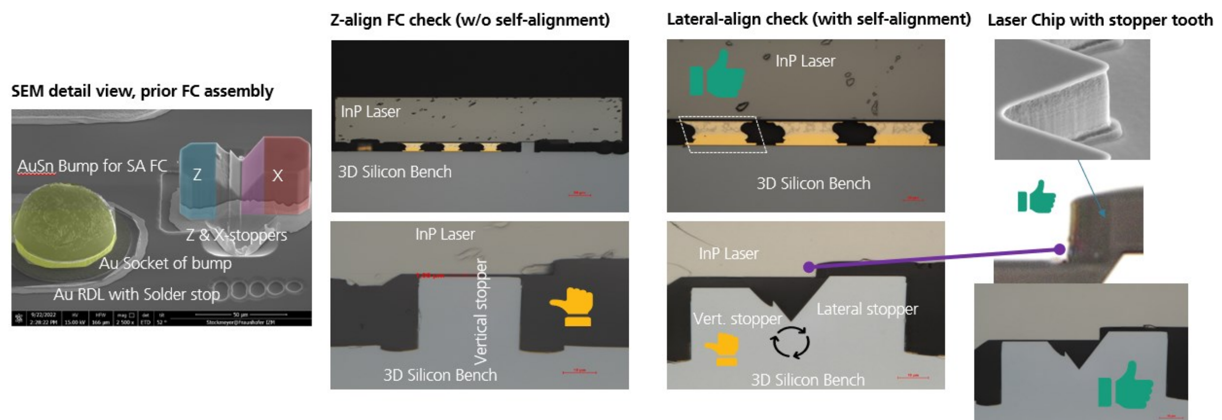


Figure 35: Flip chip Self alignment results @ M42 (Cross-sections)

Task 4.3 Bonding technologies for sensitive optical components

In this task 4.3, wafers were processed in view of preparing WP5 / hermetical sealing of fully functional microbolometers. Figure 36 gives an overview of the general workplan.

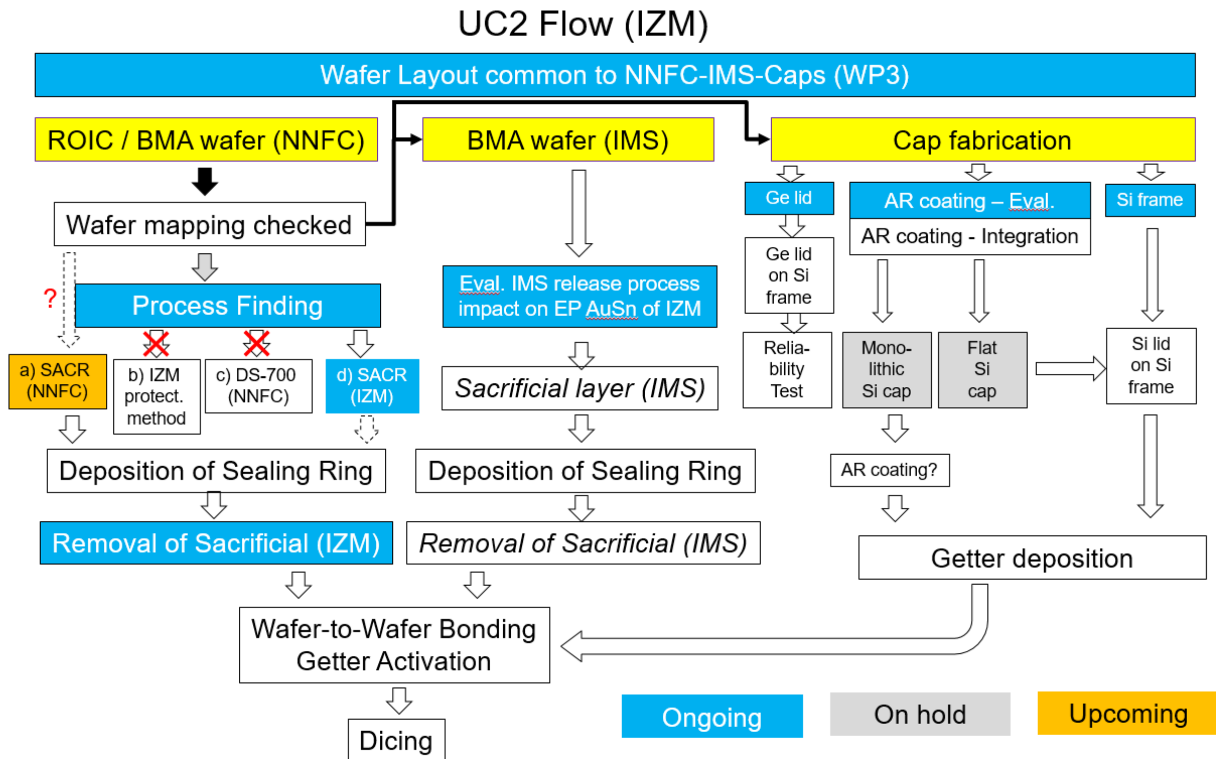


Figure 36: General Flow Diagram UC2 (IZM @ M20 / End 2020)

The Figure 37 below recapitulates the retained packages topologies and the corresponding parts needed for performing the corresponding wafer level packaging, each wafer type being labelled by a letter (A to E).

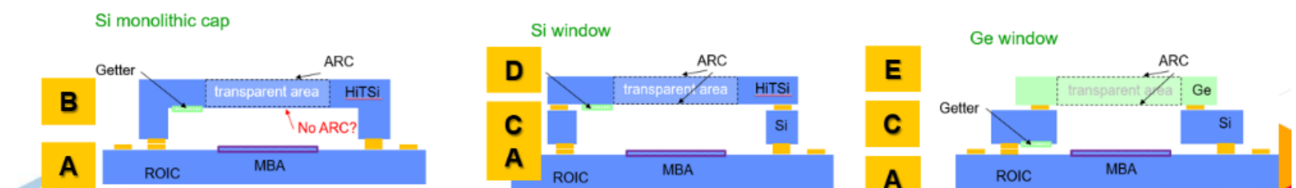


Figure 37: Three WL package topologies

WP4 grade bolometers are test wafers, WP5 grade relates to functional parts (Bolometers MEMS under fabrication at IDEAS/NNFC and FhG-IMS). Capping parts for WP5 enclose additional features, an ARC (Anti-reflection Coating) and getter, and are fabricated in high IR-transparent Silicon grade.

4.3.1 a) Sensor-Wafer preparation

Metallic sealing is targeted for hermetical bonding of the cap window onto the bolometer device. Different process flows have been drafted depending on the four cap topologies considered. The main bonding technology being considered for the wafer level capping of the bolometer structures on ROIC wafer is Transient liquid phase bonding (TLPB) with gold-tin (AuSn)

metallurgy. This relies on the formation of an AuSn20 eutectic (i.e. a molten "phase") being transformed into a single higher remelting metallurgical Au_5Sn phase so that the sealing rings do not remelt during typical solder SAC reflow, which should permit next level integration without deteriorating the sealing of the package, a.o. due to thermal budget in subsequent integration levels (no remelt of the sealing join). Thermocompression bonding was also optionally considered at project begin to seal the cap with the ROIC device using gold rings instead of AuSn solder-based rings, but had to be withdrawn to limit the work load vs. COVID-19 situations.

Following major processes are required for the preparation of the Sensor Wafer:

1. Local structuring (opening) of release layer (supported by means of lithography structuring and plasma etching)
2. Electroplating Deposition of sealing ring structures (Gold or Gold-tin, still to be defined) in semi-additive process, supported by means of Sputtering (adhesion/barrier/seed layers) and lithography processes and etch removal of sputtering layers,
3. Electroplating / Deposition of stoppers in a similar manner, supported by means of lithography processes,
4. Entire Release of Microbolometer MEMS Structures
5. Annealing for degassing
6. Wafer bonding with capping counterparts

Compatibility of the MEMS release layer is a key point for back-end processing. This release (also called sacrificial) layer, processed by bolometer supplier/fabricant, not only permits to fabricate the MEMS membranes forming the bolometers, but also protects them by bringing mechanical support or even embed them for protection of their upper surface. This item is a predominant/impacting aspect, which determines the most adequate process flow for correct wafer preparation, not only for the sensor itself but also the different capping counterparts to be bonded on. Especially regarding compatibility with back-end wafer level processes in place at Fraunhofer IZM (for example, compatibility versus resist processing for photolithography processing).

Effectively, in order to carry out back-end, the thin bolometer MEMS membranes must be constantly protected over all the different process steps and the release of the layer must be compatible with the performed back-end preparation. However, during 2020, it figured out that the MEMS Fabricant of IDEAS (NNFC in South Korea) withdrew its sacrificial material and could not anymore deliver bolometers with the first-expected sacrificial layer, due to process stop at their fabrication site.

Apart of this, extensive basic trials were also necessary to even find a way to proceed with this unknow / external material composing the release layer.

Three options were identified as illustrated in Figure 38:

1. The first one relies on a proposition of IZM to apply a sacrificial release layer by their own, since the original sacrificial layer cannot be anymore provided by the MEMS fabricant. This means that the MEMS are delivered fully unprotected and that Fraunhofer IZM must develop a new process to sustain ("underfill-like") and protect the very thin MEMS membranes, without damage, collapse nor bend of the membranes, with a 2 µm gap between MEMS plates and ROIC.
2. The second one foresees, the original sacrificial layer is back at the MEMS fabricant and is compatible to all processes at Fraunhofer IZM, including wet processes (lack spin, lack removal, and related solvents as well as plating bath), without mechanically

damaging nor chemically damaging the exposed MEMS membranes as well as the sacrificial layer itself. This is very unsure, since the sacrificial layer is a non-identified / unknown external material at Fraunhofer IZM (not in process program)

3. The third relies on the applying an overdeposition with a material of IZM, embedding the MEMS, themselves sustain by a sacrificial layer provided by the MEMS Fabricant/provider.

All the three options also imply that the removal of sacrificial and/or protective layer does not affect the MEMS. Most naturally and preferred version would be the use of the original sacrificial layer, since the fabricant must know how it behaves/impacts in respect of the MEMS functionality, nevertheless its compatibility could not be fully assessed within the IZM process flow.

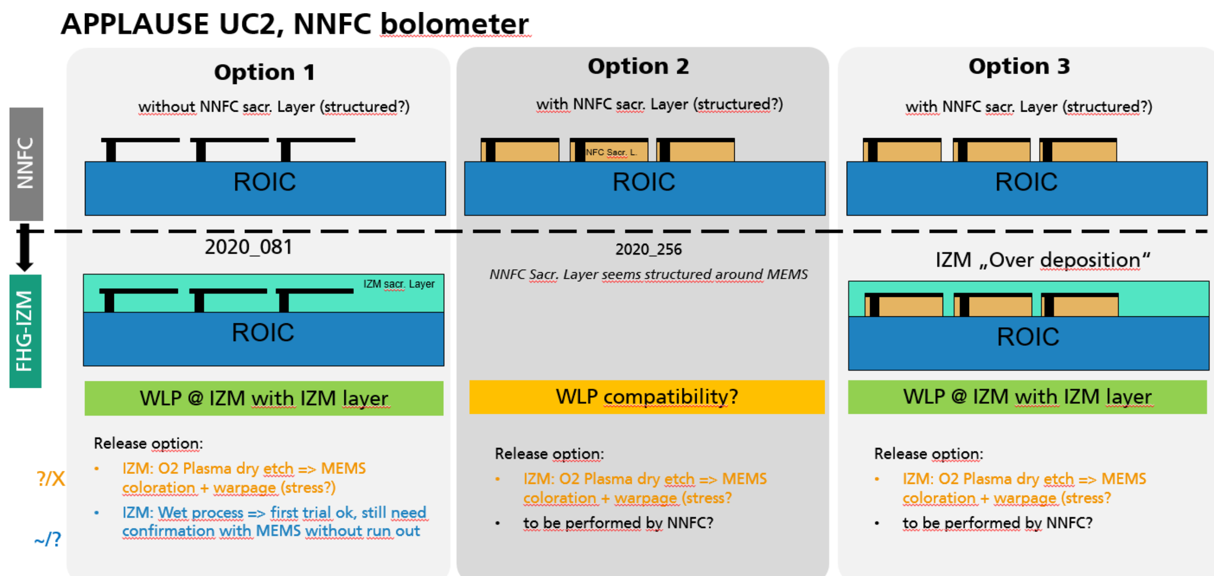


Figure 38: Interfacing delicate Bolometer MEMS with Wafer Level Packaging

The option 1 and 3 were then retained and tested, not only for applying the over-protective layer but also to remove it safely.

In option 1, process finding regarding applying and removal of a sacrificial/protective layer prepared by IZM were performed with NNFC shortloop wafer delivered by IDEAS with free-standing / unprotected bolometers. Here IZM tried to apply a layer “embedding” the thin MEMS membranes, to 1) mechanically sustain the thin membranes having a 2µm gap to substrate and 2) to protect the bolometer MEMS top surface during processing of the bolometer wafers at IZM. The results were at first sight positive, however, all results were jeopardized, since it appeared in retrospect that the provided wafer material was partly defective, with MEMS membranes already stuck down or even crashed. A precise statement on the performed processes with Fraunhofer ZM material for sacrificial layer, if affecting the tiny MEMS-Membranes (up or stuck down), could not be done (Figure 39). A methodology of precise inspection of specific MEMS membranes was took in place afterward to leverage this point for further works.

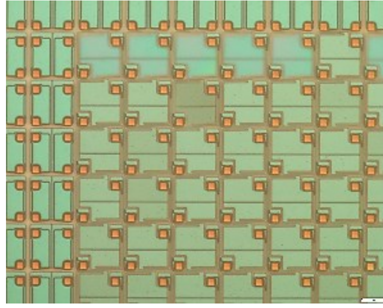


Figure 39: Short loop Bolometer Wafer of NNFC/IDEAS with sacrificial layer applied by Fraunhofer IZM. Some MEMS are stuck down.

Since the original sacrificial layer applied by the bolometer manufacturer NNFC was again available (Oct. 20), a second track was reopened with option 3, starting with wafers with the original sacrificial layer as originally planned (NNFC sacrificial layer) and only under the MEMS, with surrounding free of it for fabrication/electrodeposition of metallic bond rings. The purpose was 1) the testing of feasibility of removal tests at IZM and 2) to evaluate if those wafers are compatible with wafer level processes of IZM, especially lithography and the deposition of the bondrings by electroplating.

The results of all the different tests revealed that option#3 was the most promising (less-risky) for handing over IDEAS/NNFC bolometer wafers to IZM for wafer level processing and packaging of the MEMS-based sensor. A process method has been here found to keep the MEMS membranes safe over the Back-End processing at FhG-IZM.

Those assessed process developments should have been used for post-processing of functional bolometers within WP5. Nevertheless, functional wafers (WP5) could not be provided by IDEAS to FhG-IZM, due to low yield in MEMS fabrication by IDEAS subcontractor NNFC. Test wafers with bolometer MEMS from IDEAS/NNFC have been processed, results are reported below in WP5 / T5.2.2 Microbolometer preparation.

Test Wafers from FhG-IMS with only IMS sacrificial layer material ("IMS_s") and dummy MEMS ("IMS-MEMS-Dummy ") have been also processed for interface/ process compatibility testing. The IMS sacrificial layer and its release was compatible with the wafer process of FhG-IZM.

Wafer bond were performed with all those base wafers with cap wafers.

4.3.1 b) Silicon Frame Wafer

The silicon frame wafer is an intermediate part between the ROIC/MBA wafer to bond the flat germanium window. It permits to create and adapt an internal volume for vacuum sealing which else would be too small by bonding directly the flat lid/window onto the microbolometer. Germanium and silicon lids were similarly bonded on the silicon frame and then compared in terms of characterisation/failure (WP6).

The fabrication of the silicon frame on 200 mm wafer (Figure 40) consists in general onto electrodeposition of the bond rings on both sides and etching through the silicon over the place where the pixel matrix of the MBA is.

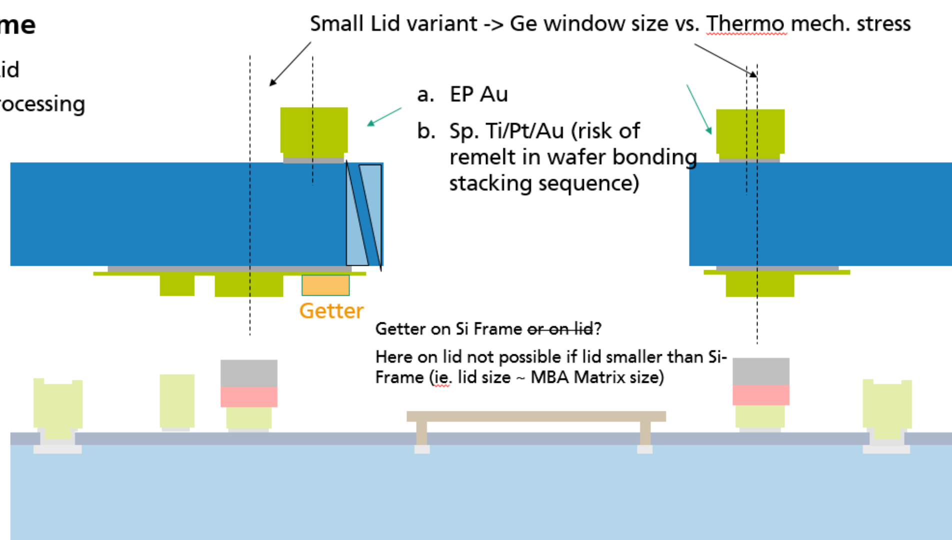


Figure 40: Silicon frame wafer with through DRIE etched cavity

Fraunhofer IZM fabricated silicon frame wafers by silicon dry etching (Figure 41). The Silicon Frame includes gold bond rings on its both sides (Front and backside) for joining with AuSn bond rings (processed on Silid and Base/device wafers). Those Si-Frame wafers were first bonded to silicon lids and then to base/device wafers.

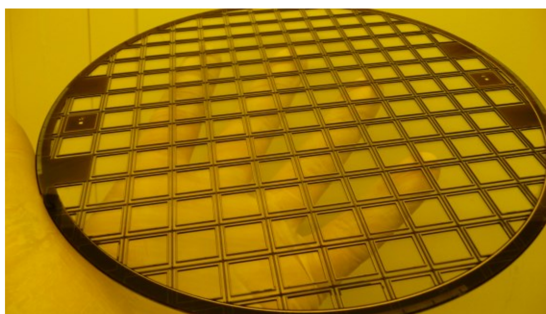


Figure 41: Fabricated Silicon Frame wafer,200 mm, prior wafer bonding with Si Lid

4.3.1 c) Reconfiguration of Germanium Windows (and Silicon Lids)

- Germanium lids

After discussions with UC2 leader IDEAS, silicon capping has been considered as more straight forward regarding the system and packaging. Germanium remains a candidate but as explorative work due to heavy concerns on high CTE mismatch with silicon.

Despite of the concerns, Germanium wafer in technical/mechanical grade were purchased for evaluation purposes. A process flow was drafted for preparation of seal bond rings, dicing and reconfiguration of Si and Ge Windows chips on a temporary carrier.

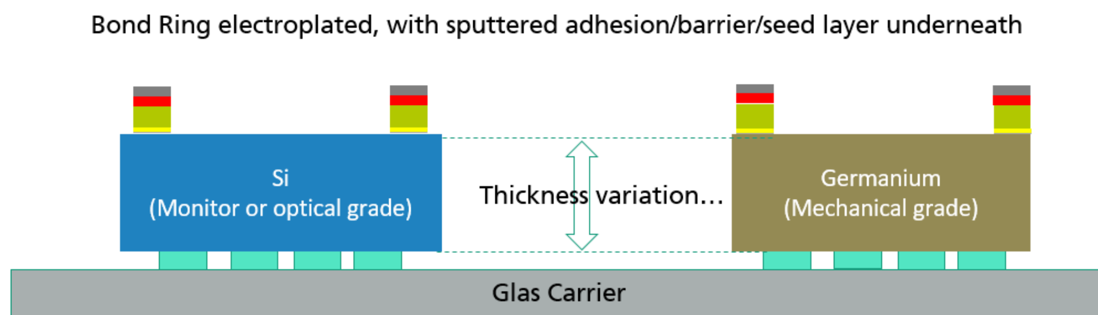


Figure 42: reconfigurated Silicon and Germanium windows

Processing of the reconfigurated Ge and Si windows (Figure 42) consists mainly in electro-deposition of Au (or AuSn) bond rings for sealing on Ge and Si wafers, Stoppers for wafer bonding, dicing of the wafer, reconfiguration of singulated parts on temporary wafer for wafer-to-wafer bonding onto Si-Frame wafer and then onto ROIC/MBA Wafer.

- Die level lid (germanium) (label E, fig. 12)

Ge Lids were prepared with AuSn bond ring from 6'/150mm Ge wafers for bonding to 8'/200mm Si-Frame Wafer. Due to wafer size (and CTE mismatch to Silicon), the Ge Wafers have to be diced in single lids, then to be reconfigurated on carrier to adapt the wafer size and grid.

For this, dedicated 200mm temporary carriers have been fabricated at Fraunhofer IZM (Figure 43) for the reconfiguration of single lids and subsequent wafer level bonding and clean carrier debonding.

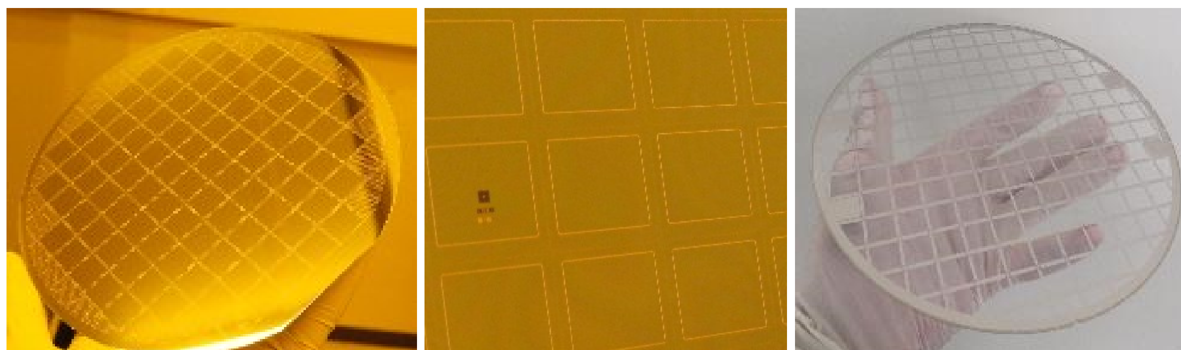


Figure 43: Left & Center - Germanium wafer (150 mm, 230 µm thick) processed as Lids prior singulation; right : special 200 mm carrier for wafer cap processing and reconfiguration of lids and wafer level bonding, 200 mm wafer.

Die level reflow and chip bonding tests (Figure 44) were performed using AuSn bond ring on Germanium (mechanical grade, three wafers) and silicon frames as bond substrates (having failed at through cavity silicon etching). The AuSn reflow depicted correct composition (ie. enough eutectic part) on only one of the three germanium wafer with rounding of the solder (Figure 44, center left), the two other wafers presenting fully insufficient melting behavior or insufficient total height. After chip bonding, due to overlapping of Au-based rings on the Si-frame top and bottom side (from layout), the sealing quality can only be partly inspected by X-Ray microscopy in tilted angle (part of WP6). An example is given in Figure 45/left.

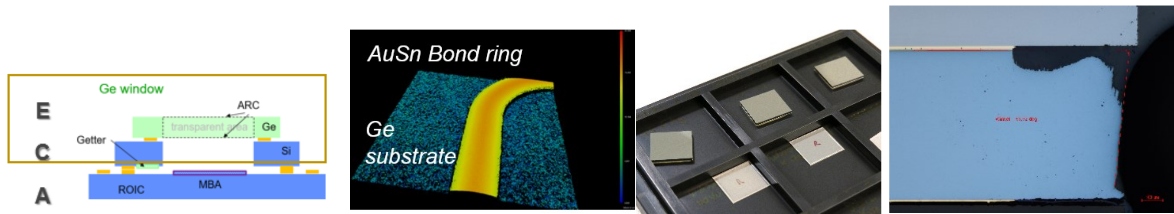


Figure 44: Package topology Germanium on Si frame in (E: Ge Lid, S: Si-frame, A: bolometer), re-flowed AuSn Ring on Germanium lid, and die level bonded germanium lids on Si-frame with cross-section.

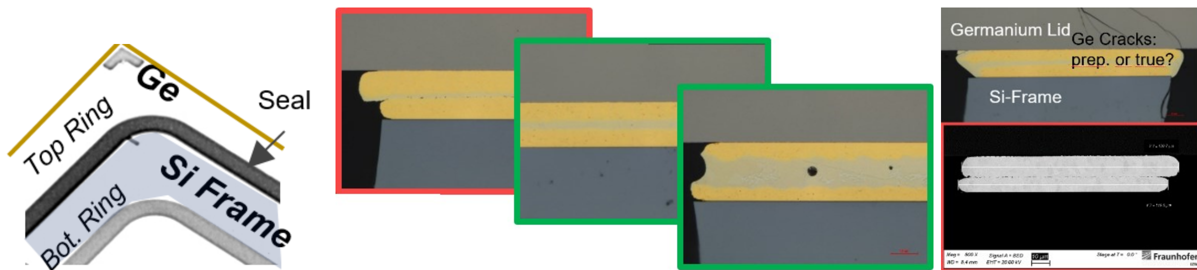


Figure 45: Left: X-ray inspection of single Ge-lid bonded with AuSn ring on Si-Frame in tilted view, Center: cross sectioning of sealed ring of three germanium lids of 3 different Ge Wafers, Right: Cross-section with crack in Ge (top), SEM of AuSn seal with insufficient solder amount (bottom).

Many cracks are visible in cross-section in Silicon or/and Germanium as well from top view on Germanium after Die Level Bonding, most probably due to the large chip size (~11x12 mm) combined to the difference in thermal expansion (CTE Mismatch) resulting in a very high level of mechanical stresses (as also evaluated by thermo mechanical simulations, not shown, FhG-ENAS). It leads to the conclusion that large Germanium chips are not suitable for bonding onto Silicon with AuSn. Due to these pre-results, the focus was displaced to Silicon Lids instead of Germanium lids as a countermeasure.

After official project end, remaining most adequate (in respect of deposited Au/Sn layers) Ge-Lids were reconfigurated on carrier and bonded to remaining Si-Frame wafer (Figure 46, left)

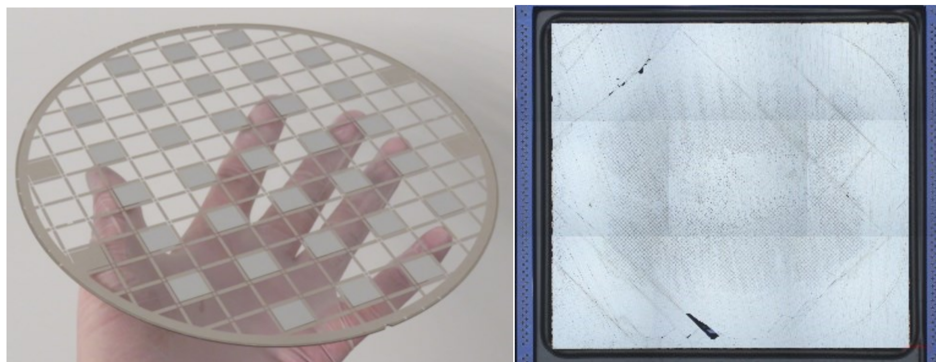


Figure 46: Reconfigurated (1:4) Carrier with single Ge-Lids (left) and cracks in Ge-Lids after AuSn Wafer bonding to Si-Frame Wafer

Apart from some post bond misalignment between Lid and Siframe, the Germanium parts were all presenting fractures and cracks ((Figure 46, right), similarly to the chip level trials. This result definitively rejects the feasibility of bonding large Ge chips to Silicon substrates using AuSn bonding and peripheral rings.

- Silicon lids & silicon monolithic cap

Wafer for Silicon lids (to be bonded with Si-Frames) were prepared for AuSn wafer bonding, inclusive integration of getter material (subcontracted to SAES).

Singulated SiLids were also reconfigurated (Figure 47), prior joining to Si-Frame.

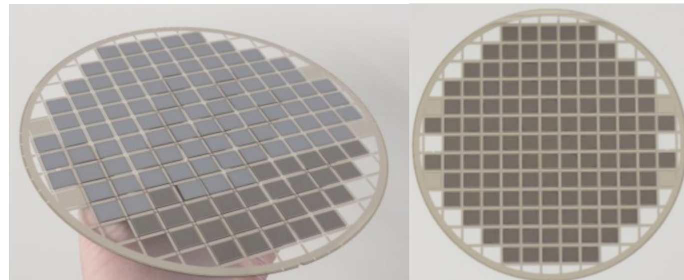


Figure 47: SiLids reconfiguration (picture left, single lids originating from two different SiLids wafers)

- Silicon monolithic cap.

For the purpose of UC2, European providers of optical grade silicon wafers for the silicon cap material (ie. compatible for IR applications, low absorption around 9µm) as well as anti-reflection coating for silicon substrate have been identified and contacted. Depending on their capabilities (Si optical grade in 200 mm with AR coating, double or single sided) and the interactions with the envisioned process flows for the cap fabrication and sealing at IZM, it will further steer and determine the cap process flow and related topology to be implemented.

A monolithic silicon cap wafer (Figure 48) is in between also considered, which will comprise the Anti-Reflective Coating (ARC) on its outer side, electrodeposition of the Au sealing bond ring, Stoppers, etching of cavity by DRIE, deposition of ARC inside the cavity, getter deposition, pre-dicing, and finally wafer bonding to ROIC/MBA Wafer.

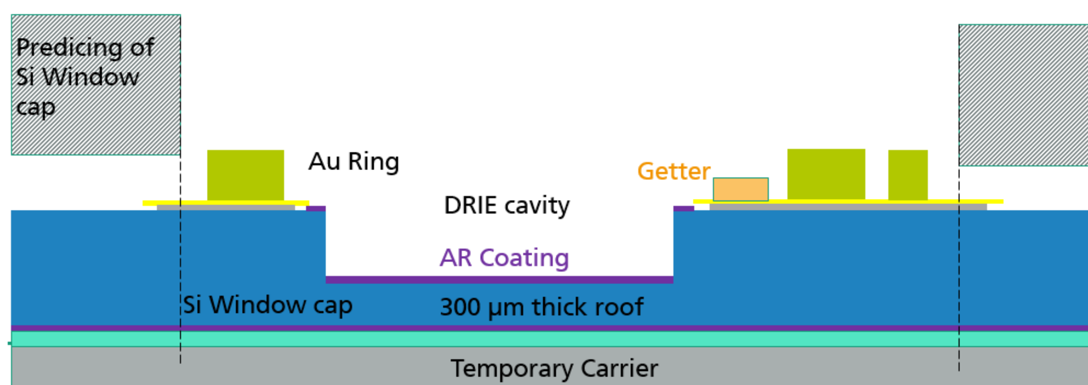


Figure 48: Concept of monolithic silicon-based cap

Silicon wafers for monolithic cap were fabricated (Figure 49) by means of lithography technics combined with additive (electrodeposition of metal rings) and subtractive processes (Si plasma etching Bosch Process, wet etching of metal layers), inclusive trials to improve the etching quality of the deep cavities over the 200 mm wafer (tuning of etch depth to reduce the dispersion/deviation over the wafer around +/-10 µm, activity WP5-level).

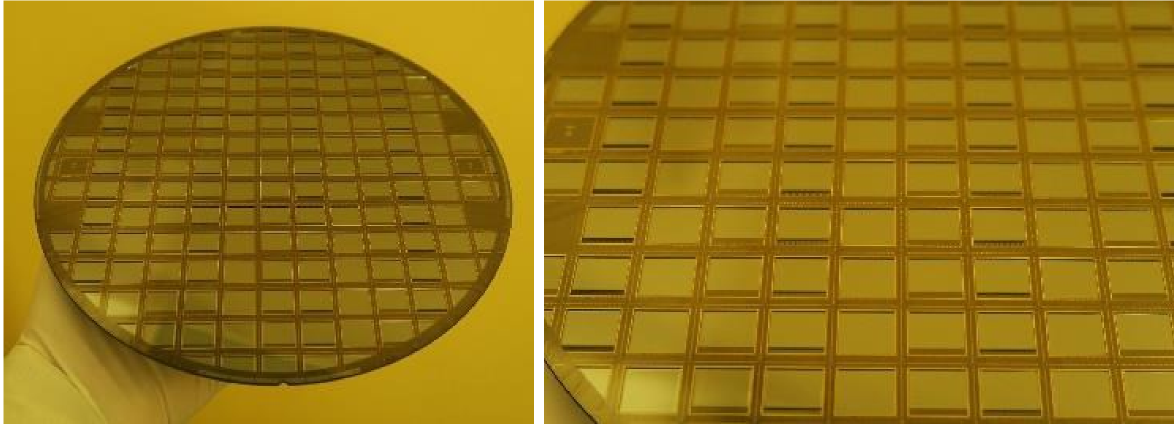


Figure 49: Silicon monolithic cap wafer, with 350 µm cavities and getters, before bonding to device wafer.

4.3.1 d) Bonding of 3-Stacked Wafers

After the individual preparation of the packaging parts, wafer bonding was performed to stack and seal the different parts together. In the case of the monolithic Silicon cap, the gold bond rings were sealed with the AuSn ring on the bolometer under vacuum chamber into the wafer bonder (Figure 50).

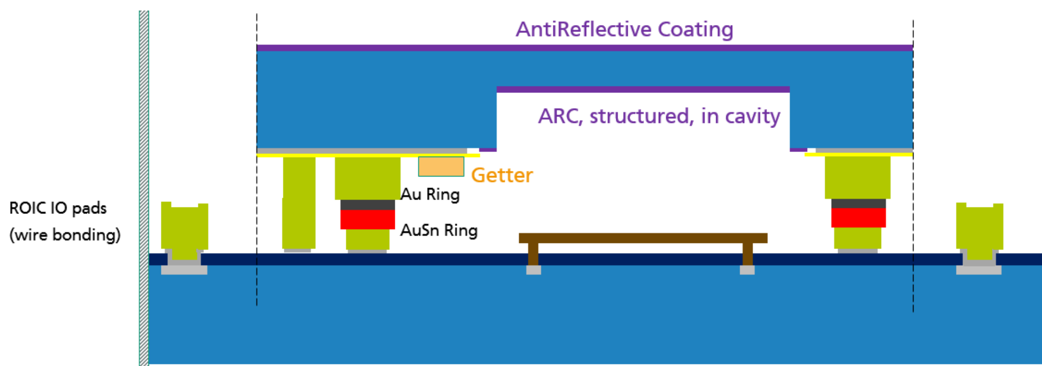


Figure 50: Monolithic Silicon cap bonded on ROIC/MBA wafer

In the case of the silicon frame, two bond sequences are at this stage under consideration, where the reconfigurated windows are first bonded with the silicon frame, this stack being then bonded further on onto the ROIC/MBA wafer, or the other way around, with first the silicon frame bonded onto the ROIC/MBA and then capping with the reconfigurated window (Figure 51).

C. Si Frame

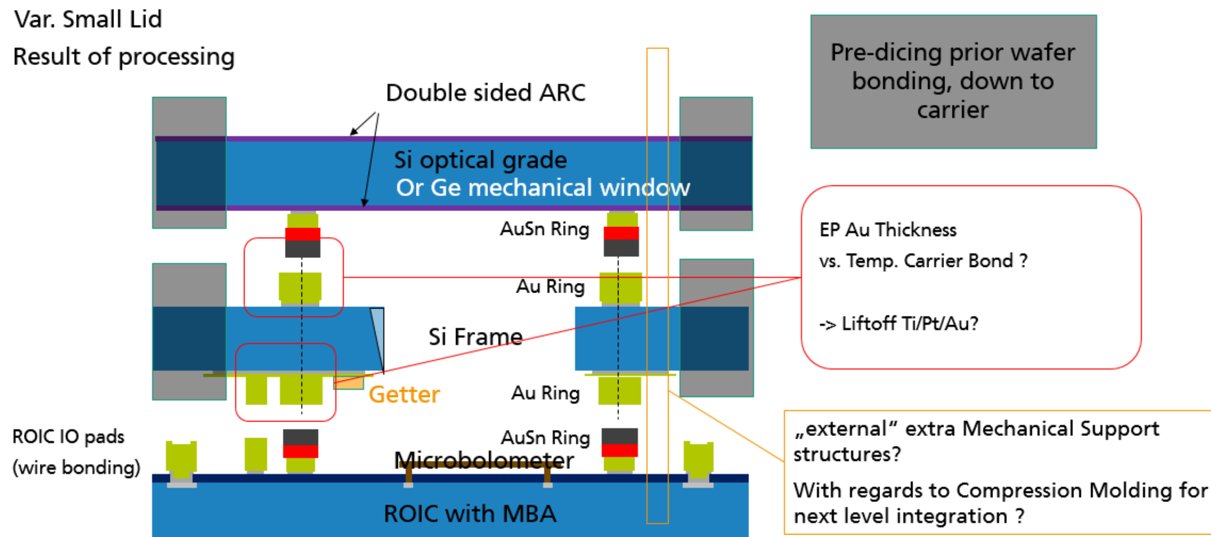


Figure 51: Stack of ROIC/MBA wafer, silicon frame and reconfigurated Windows (silicon or Ge)

The first W2W bonding attempt (Frame to Lid) was not promising but permits to identify few blocking points (Figure 52). The poor post bond misalignment leads to narrow bond line at the corners of the bond ring. None the less, the visual observation of both wafer outer sides reveals some silicon bending (deflection on Si lid side and on residual silicon membrane in the frame), sign of a possible seal. The wafer stack was not further investigated, since of low value.

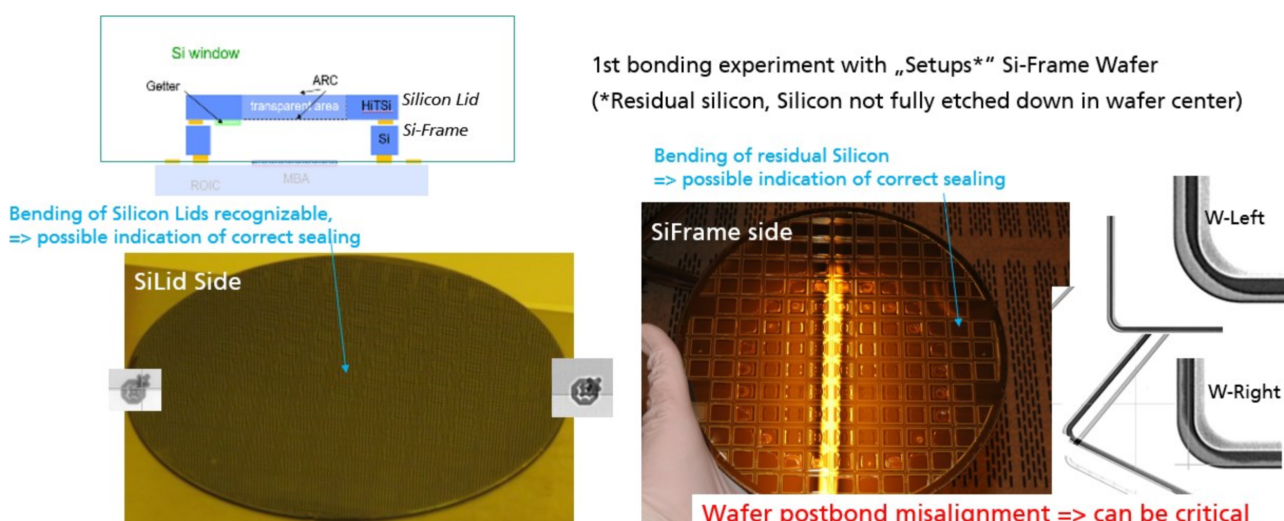


Figure 52: First Trial of W2W Bonding of Si-Lids and Si-Frame

The bonding process was then improved, especially the pre-bond preparation of the Silicon-Frame and the alignment procedure (Figure 53). The post bond X-Ray inspection of the wafer stack is satisfying, both wafers are still correctly aligned and the rings seem all to be bonded, the ring corners do not display particular risk of leakage, and even the bonded rings seem to have less voids than in the other wafer bond. No destructive physical analysis has been performed, the Si-Window will be first bonded to a bolometer/sensor wafer (test or functional).

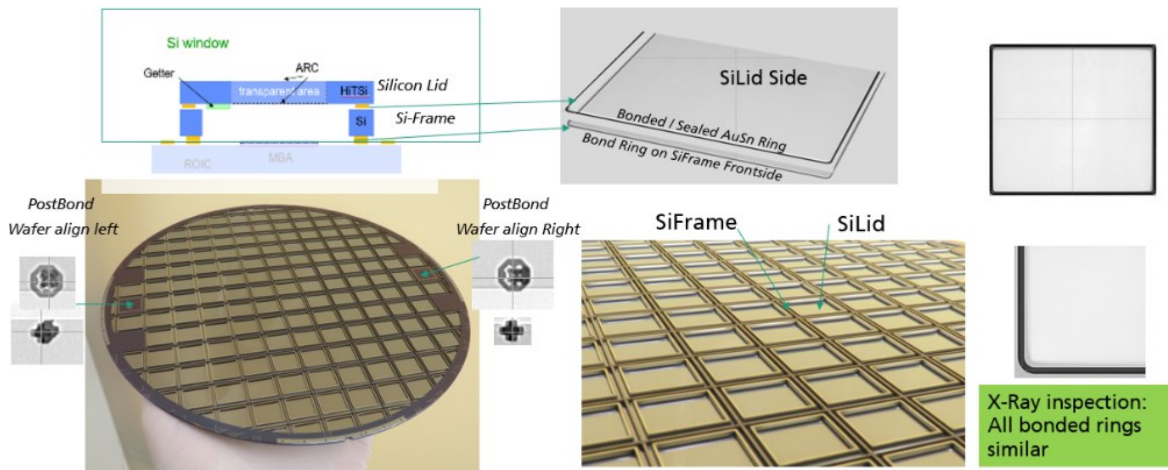
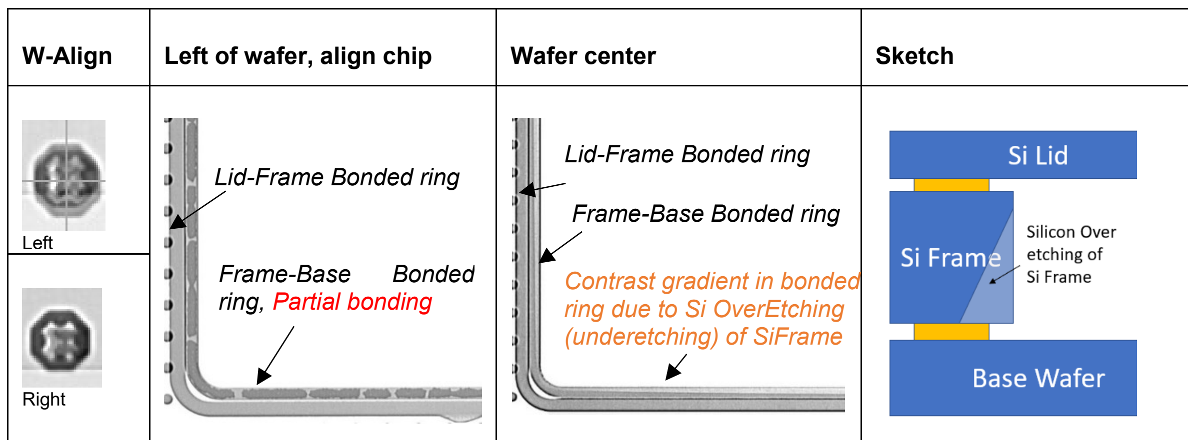


Figure 53: Fabricated Silicon Window with improved W2W AuSn bonding process (HybridCap#02)

Having achieved the first "stage", the silicon window wafers (also called hybrid cap, consisting of SiFrame bonded to Si Lid Wafer) were bonded on the base/device wafers.

The results were partly satisfying: the first bond test to a base wafer (with the hybrid cap of Figure 53) was encouraging: despite some unbonded ring areas (Figure 54, left) and silicon over etching of the Si Frame backside (Figure 54, right), the bond rings to the base wafer were generally sealed.



W-Align	Left of wafer, align chip	Wafer center	Sketch
Left Right	*Lid-Frame Bonded ring* *Frame-Base Bonded ring, Partial bonding*	*Lid-Frame Bonded ring* *Frame-Base Bonded ring* *Contrast gradient in bonded ring due to Si OverEtching (underetching) of SiFrame*	Si Lid Si Frame Silicon Over etching of Si Frame Base Wafer

Figure 54: X-Ray inspection (example) after bonding of HybridCap#02 on base wafer. Picture Left: ChipAlign Left & Picture Right: Wafer center

After removal of Si Lid Carrier, 81 of 123 devices were still sealed after "double AuSn bond" (Figure 55), i.e. ~66% sealing yield (based on silicon lid deflection).

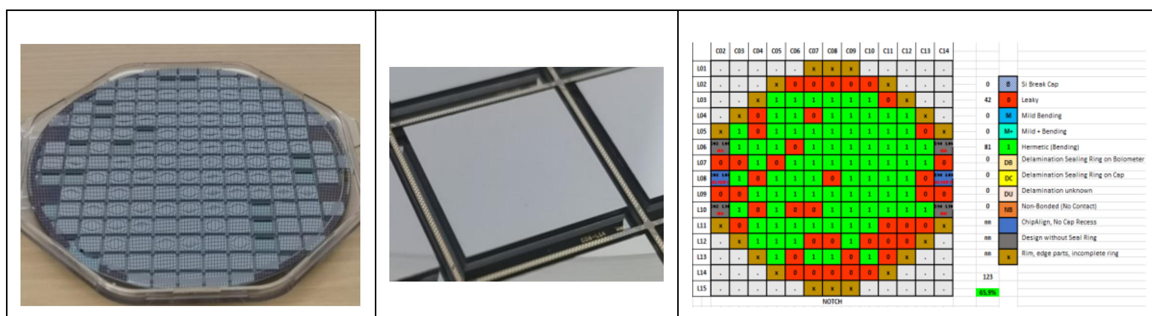


Figure 55: HybridCap#02 bonded to device wafer, after 1 year ambient storage

However the other bonded hybrid cap (#03,#04,#05) revealed some misalignment and/or incompletely sealed rings to the device side, already during bonding between Lid and frame. The bonding to Pirani MEMS wafer (base/device wafer) was then unsatisfactory.

Wafer bond trials with cap wafer (see below and task 5.2.3) leaded in general fortunately to better bond results (Figure 56), i.e. higher yield up to 80% in WP4, since only one wafer bond is involved for wafer sealing.

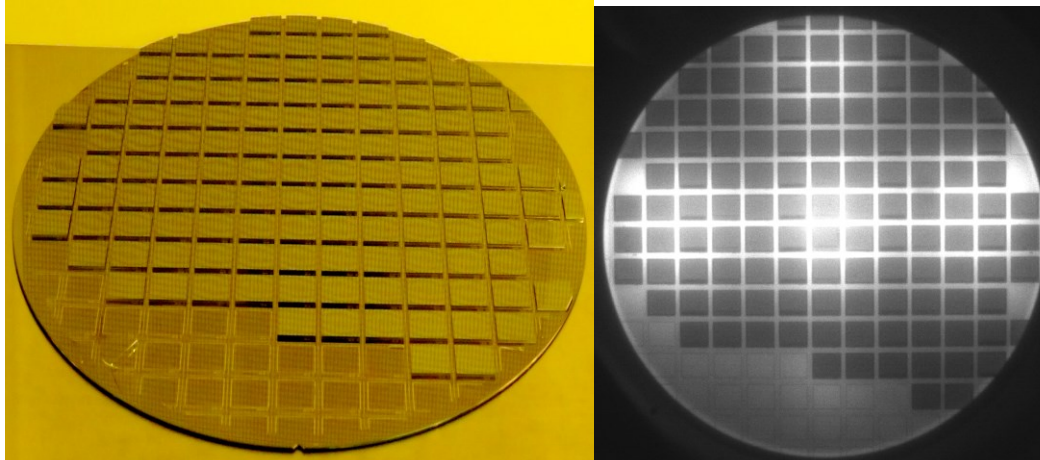


Figure 56: Macro-inspection after Wafer bonding and Carrier release of monolithic cap: silicon deflection (left) and IR-Photography (right)

T4.3 - Summary

Wafer level bonding with AuSn technology was performed:

- to bond (seal) base device wafers with monolithic cap wafers, for bonding setups
- to seal SiLids with SiFrames, creating hybrid cap wafer
- and then sealing the hybrid cap to base wafer

inclusive dicing of cap wafer and base wafer. Figure 57 recapitulates the WP4 works and main results. Bond results were evaluated by X-ray inspection and yield estimation performed by observation of Silicon bending on cap side. A yield over 80% could be reached in process setups, inclusive cap and base wafer dicing.

The reason for yield “loss” is in between also identified and mostly related to handling of cap wafer and some adhesion issue of the electrodeposited bond rings to the bulk silicon.

The different sealing WP4-level trials fulfilled entirely their aim with support for WP5, for successful sealing results in WP5.

In the frame of WP5, functional Pirani MEMS wafers from IMS were sealed for evaluation of residual pressure (vacuum level/quality) inside the WL packaged devices (collaboration work with IMS and USN, paper presented at ECTC2023).

The EU Report/Deliverable D4.3 - Bonding Processes - gives further insight on the work performed.

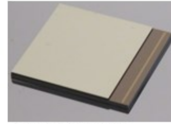
Wafer Level Packaging for thermal imaging MEMS-based sensors

In collaboration with: ideas Fraunhofer IMS

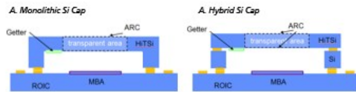
I. Background / Goal

Wafer Level Packaging for large MEMS array IR Sensors

- **Silicon Cap fabrication, incl. :**
  - Metal bond rings for hermetical sealing
  - Anti-Reflective Coating Intergation
  - Getter Integration
  - Cavities of different sizes
- **Bolometer MEMS Back-End**
  - Metal bond rings for hermetical sealing
  - Processes compatible with fabricated MEMS
- **Processes compatible for low vacuum encapsulation**
- **Wafer-to-Wafer vacuum encapsulation**



Full processed Test-Vehicle



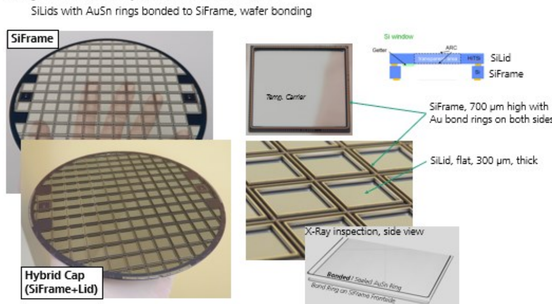
Two different cap topologies for WLP

II. Silicon Cap Fabrication

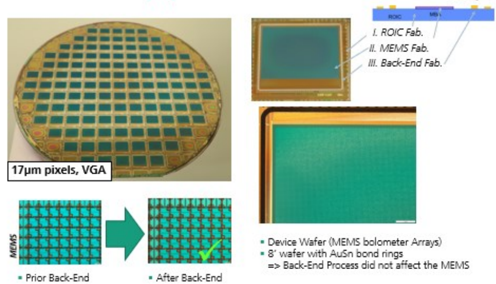
A. Monolithic Silicon Cap

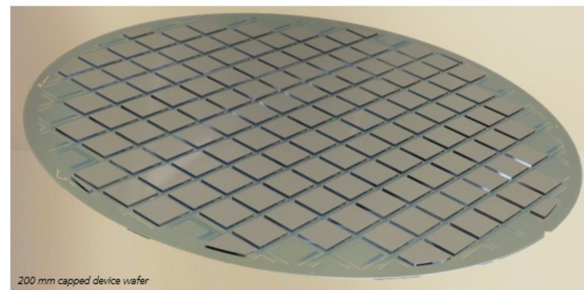
B. Hybrid Silicon Cap, for extended volume

SiLids with AuSn rings bonded to SiFrame, wafer bonding



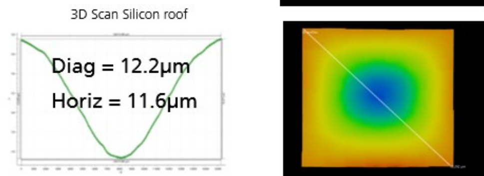
III. Bolometer MEMS preparation





IV. Wafer Level Vacuum Encapsulation

- **Process development using evaluation of deflection of Silicon roof**



A. Wafer bond process setup

B. Including dicing cap and bolometer

South: BREAK in handling

AuSn Bonding after W2W sealing

Device Wafer (Bolometer short loop)

C. Process Correction/Amelioration

AuSn Bonding after W2W sealing

Si Cap

Device Wafer

Increasing complexity

D. Full scale W2W capping

NEXT: **Wafer Level Demonstration with MEMS Pirani device Wafers for vacuum level evaluation**

Figure 57: Overview T4.3 activities, results and migration to WP5 / FhG IZM (Poster ESREF2022, End September 2022)

Task 4.4 Medical and biocompatible photonic packaging

Fraunhofer IZM designed and started processing of a test vehicle for the several process development sub tasks of thin IC into flex integration as well as flex on stretchable integration. The test vehicle includes two dummy ICs, the MUSEIC device (to be finally provided by IMEC) and a memory chip, with the intention to mimic the final devices in pad layout and size, especially thickness.

Task 4.4.1 Technology development for flexible/stretchable substrate with very thin components

Task 4.4.1 a) Integration of thin chips in flexible polymer layers + Task 4.4.1 b) Planarization and Embedding in thin film polymer Multilayer + 4.4.1 c) Release of flexible layers of temporary process carrier

Flex embedding

The first dummy IC has the size and the pad layout identical to the MUSEIC, which has been later used in the functional demonstrators. The second IC has the size and pad layout of a typical flash memory, which is later necessary for data storage in the functional demonstrators. Both dummy ICs were grouped on a wafer layout and are under processing at Fraunhofer IZM. The dummy ICs include simple routing, IO-pads and passivation openings similar to functional ICs. The dummy IC wafers were back ground and polished down to 20 µm remaining thickness and singulated by plasma etching. The created ultra thin dummy ICs were first used for setup of the embedding process into the flex.

First, the preparation of the MUSEIC and Flash memory dummy test chips for the setup of the embedding process into the flex was carried out. The processing steps for the test chip fabrication included the deposition and structuring of AlSi RDL and pad structures, deposition and structuring of a SiO2 passivation layer with openings above the IO pads, preparation of die singulation by dry etching of streets, temporary wafer bonding as well as back grinding and polish to 20 µm remaining thickness. With the back-grinding step all dies were singulated. The wafers were then mounted with the thinned back side to tape and the temporary carrier wafer was removed and the remaining adhesive was cleaned. The process was optimized to reach close to 100 % die yield. The test chips could be picked from the tape and used for subsequent assembly setup for embedding into the high-density flex. Figure 58 show chip views and details of the MUSEIC test chip (left), a Flash memory test chip (center) as well as an image of one wafer carrying both types of test chips after thinning, singulation and carrier release.

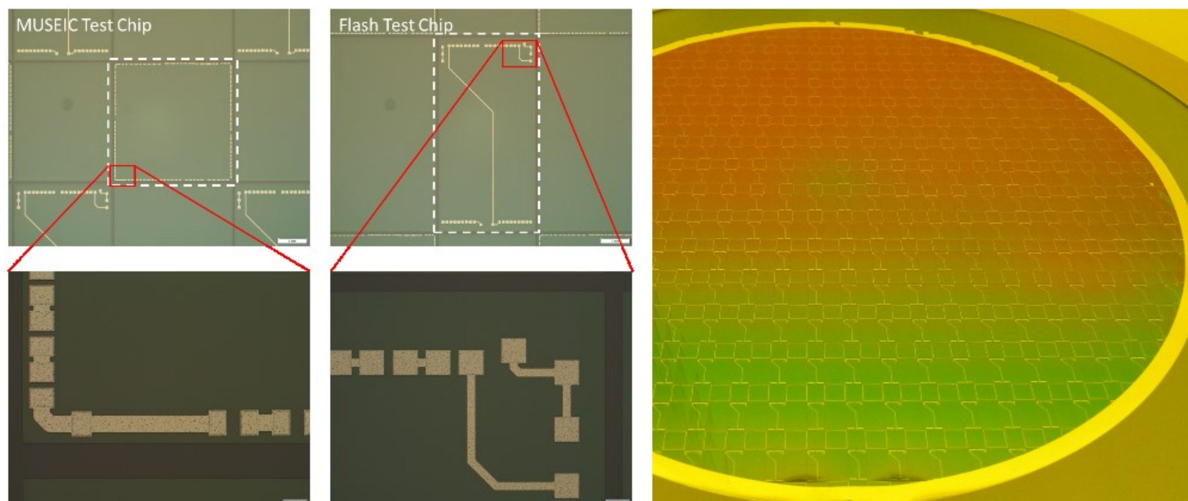


Figure 58,MUSEIC test chip (left), Flash test chip (center), full wafer with 20 µm thin singulated test chips (right) (FhG-IZM)

The availability of those test chips permitted to proceed along with the setup for their placement onto corresponding adhesive depots onto the flex base layer for the high-density flex fabrication. This flex is created using a sequential build up process of Polyimid (PI) layers on a rigid

wafer (see also process flow in Figure 60). After first placement trials, it was found, that due to the large lateral dimensions of the chips (Dummy-MUSEIC: 4320 x 4320 µm2, Dummy-Flash-Ram: 3550 x 7090 µm2), air got enclosed under the chips during the placement process, which caused extensive chip warpage and misalignment. However, both effects have to be avoided to reduce stress on the chips and to enable later a proper connection of the chip IOs which is only possible, if the chips are only slightly (<15 µm) misplaced from their expected placement position. In further trials it was tried to optimize this placement process to reduce air enclosure and die shift, with a small redesign step of the glue. Especially the MUSEIC is critical regarding to die shift, since the IO pads have only 40 µm wide passivation openings and a pitch of 55 µm. The revised process allowed a placement of the dies with sufficient accuracy, but some air enclosure is still observed. Further trials were executed with respect to further minimization of the void enclosure.

The left picture in **Fehler! Verweisquelle konnte nicht gefunden werden.** shows a MUSEIC test chip with large die shift and consequence when performing via opening. This is not acceptable since the full field mask for the photo structuring of the following polymer layer cannot accommodate the shifted die positions. The via patterns in the mask require the die to be located within minimal shift around its expected position. As can be seen, the processed vias in the covering polymer are misplaced to the IO pads. The right image shows a MUSEIC test chip with small die shift. This result could be obtained after the last optimization step. The polymer vials are well reaching their corresponding IO pads.

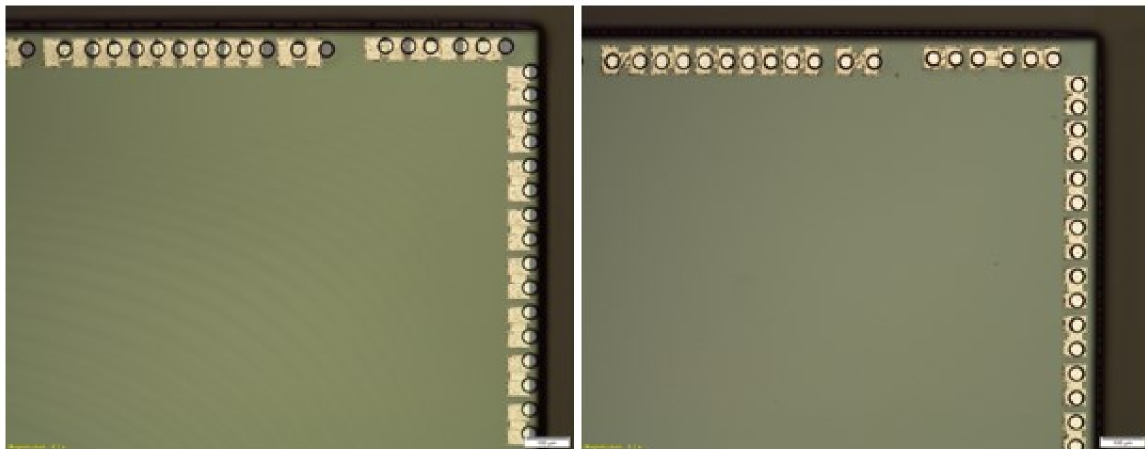


Figure 59, left: die position misplaced to position of polymer vias, right: process improved, polymer vias now fitting with IO pad positions on die (FhG-IZM)

The fabrication of the flex with the two embedded thin test chips could be then completely finished. According to the process flow given in *Figure 60*, a routing layer was created on top of the polymer, which covers the thin ICs (step 6). The routing layer was fabricated using copper electroplating from semi-additive wafer level redistribution technology. It enables high density wiring and connects all IO pads of the ICs by the vias in the polymer layer and redistributes or connects the IOs with each other or with the peripheral 2nd level IOs of the flex. A final polymer passivation layer was deposited by spin coating and lithography to protect the copper wiring and access only the peripheral IOs of the flex (step 7). Finally, the flex IOs were strengthened by electro-plating of additional 10 µm thick copper (step 8), to comply with TPU embedding process. This enables later a laser drilling process to stop on these pads when the flex is embedded into polyurethane and connected by laser drilling. The release of the layer has been performed using an excimer laser, available in the clean room facilities, by adapting the laser parameters.

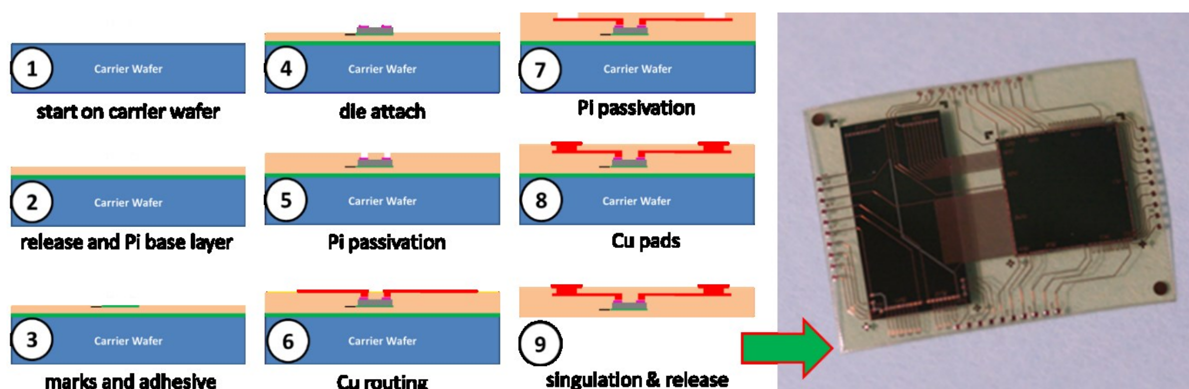


Figure 60: schematic process flow of flex fabrication with thin embedded ICs and example of flex with two embedded test chips (flex thickness 50µm, lateral dimensions 12x9mm2)

The major lessons learned from this process setup are, that test ICs can be extremely thinned and embedded into thin film flex as it was the goal in this project part. However, in order to enable this approach, the ICs need to be as small as possible and stress released so that the risk of die breakage after thinning and during die attach is minimized. This required a wafer level thinning / polishing and singulation of the ICs by plasma etching. The functional MUSEIC (WP5) were only available as already singulated IC as part from MPW (Multi-Project Wafer), so that the required wafer level preparation is not possible. The functional flash ICs were also available as a single 300 mm wafer and the dies were with 5,8 x 5 mm2 also very large.

Based on the given boundary conditions and high risk to fail, the technology approach for the functional flex module (WP5) had to be adapted/changed to a solution were the chips will not have to experience an extreme thinning for embedding into the flex. Instead of this, the ICs have been assembled onto the surface of the functional flex, the flex serving in this case as interposer/interconnect substrate. The original approach of embedding the ICs with thickness of approximately 25 µm has been partly tested parallelly, but in reduced risk, as an alternative explorative sequence, without great success.

Task 4.4.1 c) Release of flexible layers of temporary process carrier

The release layer is integrated in the flex and the laser process has been adapted from existing know-how. The release of the layer was successfully performed using an excimer laser, available in the clean room facilities.

Task 4.4.1 d) Embedding in extensible/stretchable substrate materials

TPU embedding

For the development of the embedding process in a stretchable matrix which is compatible to skin, a test design was developed allowing the same measurements of Daisy chains and contact resistance offered by the thin film test vehicle. The layout is shown in Figure 61. The test vehicles are used to develop and evaluate the assembly processes of the thin film flex face up and face down as well as the via formation process. After successful process development the test vehicles are used for first reliability investigations.

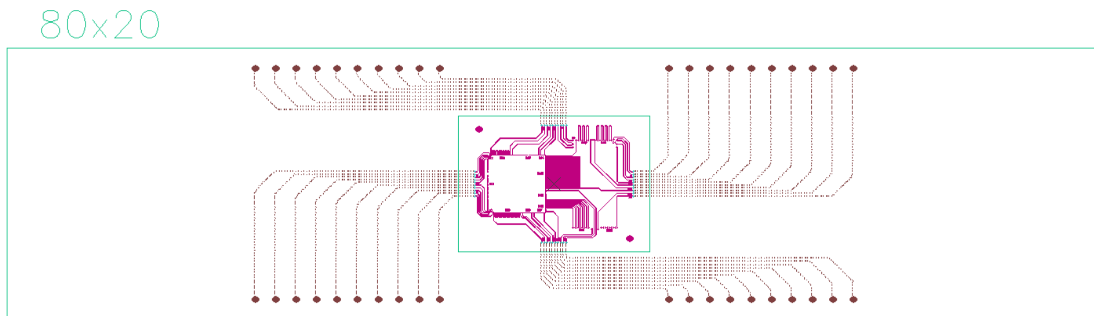


Figure 61: Test Layout for embedding in stretchable matrix with meandered Cu tracks at M12

For the embedding of the thinfilm flex in the stretchable matrix of the patch the approach of interconnection by electroplating was chosen (*Figure 62*). Later in the project an alternative approach with a face down assembly of the flex will be tested as well for WP5, as already mentioned.

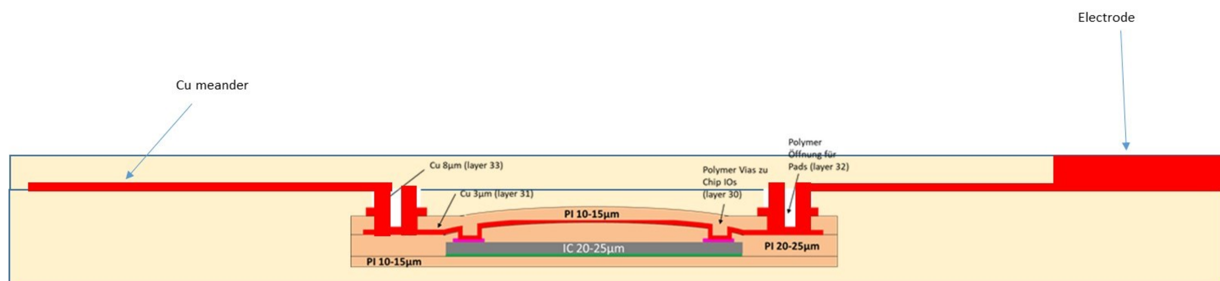


Figure 62: Principle for embedding thin film flex into stretchable matrix

For the fabrication of the final dummy patches, the process was used as shown in Figure 64.

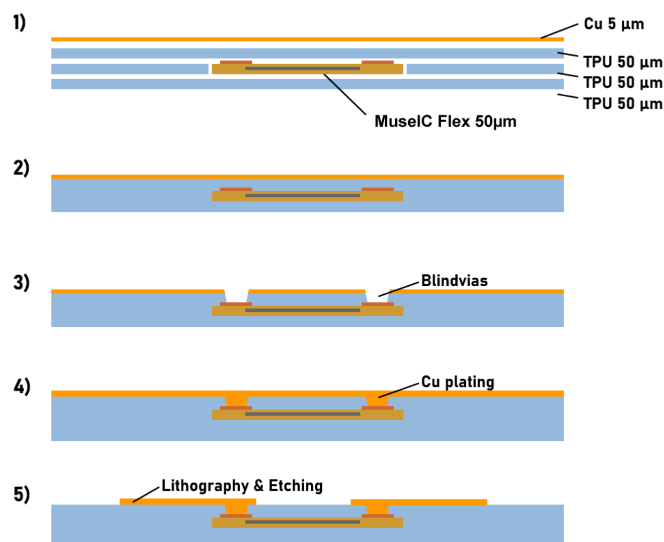


Figure 63: Process flow for generation of stretchable TPU substrate with integrated thin film flex

The process is done on a rigid carrier panel, which is not shown in the pictures. The TPU process flow starts with assembly of the thinfilm flex face up on a thermoplastic polyurethane

foil. The thin film flex is positioned on a TPU foil without metallization. Since the TPU is an adhesive, no additional adhesive layer is required. It is important that the thinfilm flex is not deformed too much. A slight bowl formation cannot be avoided and is acceptable. A 50 µm compensation layer with openings for the thin film modules is positioned over the assembly (i.e. an intermediate TPU layer with cut outs at the positions of the flex). A third, full TPU layer (50 µm thick) covered with a 12 µm Cu foil. This layer stack up is shown in Figure 63. The stack is then laminated in a short cycle lamination press (Bürkle) at 165 °C (Figure 66). Optical inspection shows that the embedded ultra-thin dies do not break during this process.

Task 4.4.1 e) Interconnection in extensible/stretchable substrates

After embedding, vias are laser drilled and metallized by electroplating. The Cu foil is then structured by lithography to form the circuit. At that point, the major challenge is the accuracy of the via position to the pads of the thinfilm flex. After lamination the thinfilm flex is not exactly at the position where it was originally placed. Therefore the position of the laser has to be adjusted. The process steps are shown in *Figure 64* but without the Cu layer on the TPU for better visibility.

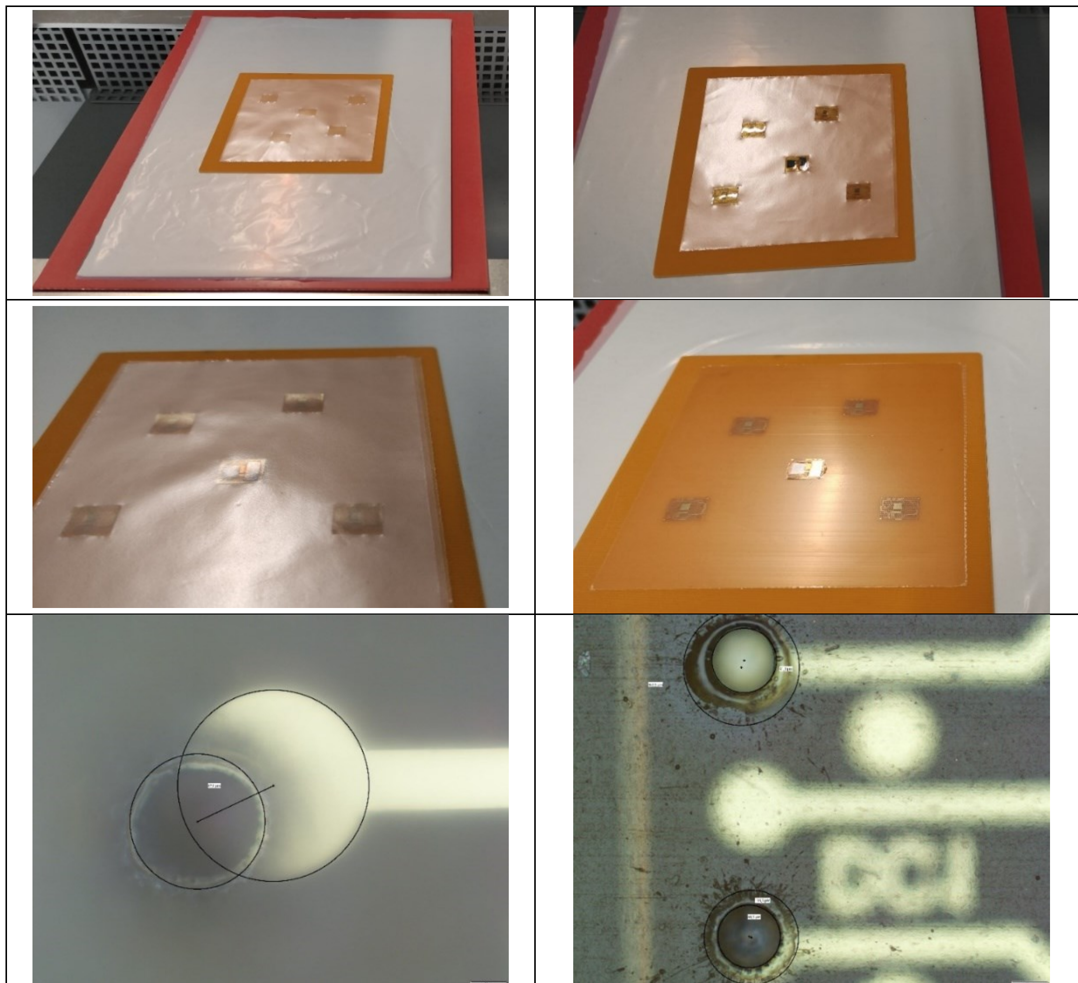


Figure 64: Process steps for embedding the thinfilm flex in TPU

The critical step is the drilling of the blind vias from the Cu side to the bond pads of the thin film flex (Figure 65). PCB-like laser drilling technology was applied with low selectivity to copper. The pad metallization on the thin film flex was realized with increased thickness of 10 µm

to provide a larger process window for laser drilling since the TPU thickness after lamination may vary slightly. The accuracy depends on the visibility of the fiducials through the TPU. The maximum TPU thickness for the blind vias is therefore limited to 50 µm. The via geometry after laser drilling is conical. The via diameter is ~80 µm on the top layer and ~60 µm on the pads of the thin film flex with sufficient accuracy. In the following step a wet chemical Pd based seed layer deposition followed by full area copper plating is done. Finally, the wiring structures are defined by photo resist and laser direct imaging (LDI), which enables to adjust the pattern to the real position of the embedded thin film modules inside the TPU stack. After copper etching and resist removal, the processing of the TPU substrates was finished and they were released from the carrier panel. A fully processed TPU substrate with embedded thin film flex is shown in Figure 66.

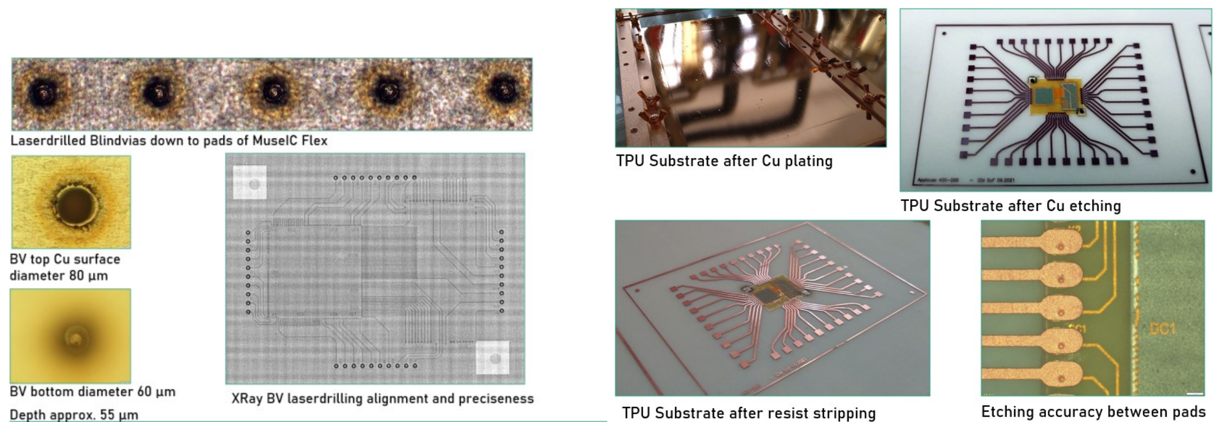


Figure 65: Fabrication of interconnects from flex embedded chips integrated into flexible TPU patch

The final resulting test vehicle is shown in Figure 66.

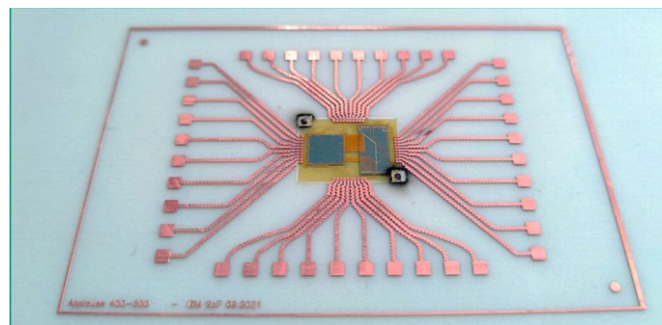


Figure 66: fully processed strechable TPU substrate with embedded thin film flex

Task 4.4.1 g) Test chips

Dummy devices were fabricated as described in T4.4.1a/b

Tests of the passive test vehicle

The process integrity was verified by electrical measurements. The embedded flex circuits carry daisy chain structures (DC1 to DC10) as well as kelvin structures (K1 to K4) for via contact resistance measurements in critical areas (e.g. die corners). The test structures are implemented between the wiring on the flex (green) ant the wiring on the thin embedded ICs (red) and can be seen in the layout image in Figure 67. The results of electrical measurements on 12 samples are summarized in Table 2.

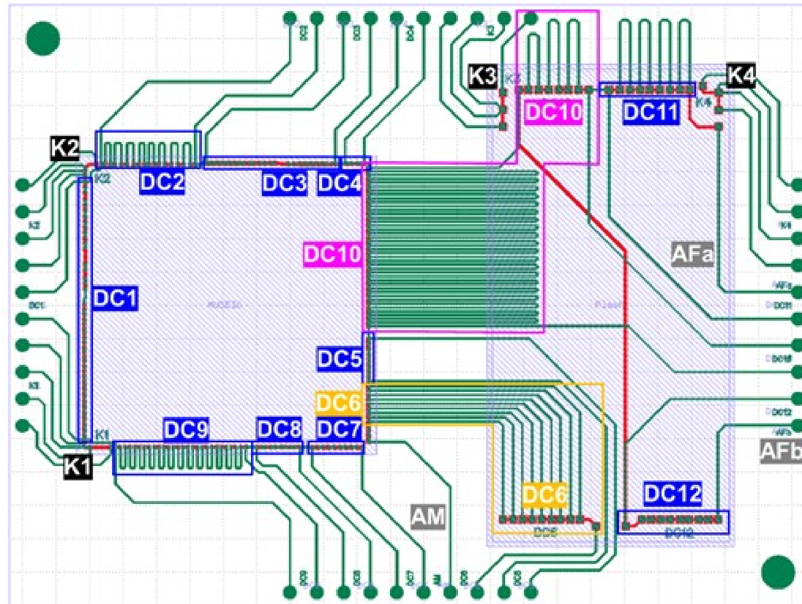


Figure 67: layout of passive test vehicle with positions of test structures

	values in mΩ				values in Ω													
	K1	K2	K3	K4	DC1	DC2	DC3	DC4	DC5	DC6	DC7	DC8	DC9	DC10	DC11	DC12	AM	AFab
Min	3,3	3,3	2,9	6,5	2,7	2,9	2,0	1,1	3,2	8,6	1,3	1,4	3,5	25,2	4,1	1,8	36,0	10,9
Max	8,1	9,8	17,2	23,9	3,4	3,5	2,5	1,4	3,9	10,5	1,7	1,6	4,2	30,6	4,9	2,2	43,5	12,0
Mean	5,4	6,9	6,9	11,0	3,0	3,2	2,2	1,3	3,5	9,4	1,5	1,5	3,9	27,3	4,4	2,0	39,1	11,4
Range	4,9	6,6	14,3	17,4	0,7	0,6	0,5	0,3	0,7	1,9	0,4	0,2	0,7	5,4	0,8	0,4	7,5	1,1
Stand.Dev.	1,5	2,1	4,8	5,5	0,2	0,2	0,2	0,1	0,3	0,7	0,1	0,1	0,3	1,9	0,3	0,1	2,7	0,4

Table 2 Statistics of passed electrical measurements of test structures in thin film flex according to picture above. Measurements taken on 12 different TPU samples with embedded flex.

For quality verification of the interconnection technology between the thin ICs and the flex as well as between the flex and the wiring on the patch, all test structures from a collection of 12 patches were electrically measured. The results of these measurements are summarized in the table in *Figure 67*. It can be seen in the statistic overview, the daisy chains for the flex to chip interconnections as well as from the chips to the outer pads on the TPU show all proper resistance values of several Ohms to tens of Ohms depending on their length. Ranges and standard deviation are small. The single measurements of the vias by using the Kelvin structures show resistances in the mOhm range as expected with some few runaways having binary values. As a first overall result of flex in TPU embedding, it was concluded, that all structures were properly connected and that all process steps appear to work at this stage. The available patches were exposed to accelerated aging and stress tests to check their robustness and reliability.

The samples were subjected to humidity tests (85°C/85% rel. hum) and thermal cycling (0..80°C). After 500h and 1000 thermal cycles the contacts in the daisy chains and 4pont-structures were all still functional without significant increase of the resistance.

During both tests a slight discoloration of the TPU could be detected. This might indicate that the material degenerated and might have changed its mechanical properties. The root cause for the behavior possibly lies in the wet chemical treatment steps during the manufacturing of the stretchable circuit boards and might be overcome by alternative chemistry.

The EU Report/Deliverable D4.6 - Report on flexible stretchable integration technologies - gives further insight in the work performed.

Task 4.5 3D-topography molding for optical component manufacturing

Next to the Si-bench, IZM explores a low-cost alternative approach of component integration for the Use Case 3 (packaging for Datacom transceivers). For this, we rely on an organic 3D freeform premold substrate with added signal routing layers, onto which components are to be placed with high accuracy.

Task 4.5 a) Process development 3D molded substrate

In order to precisely manufacture 3D freeform substrates, the focus was first put on selecting suitable materials, according to the project plan.

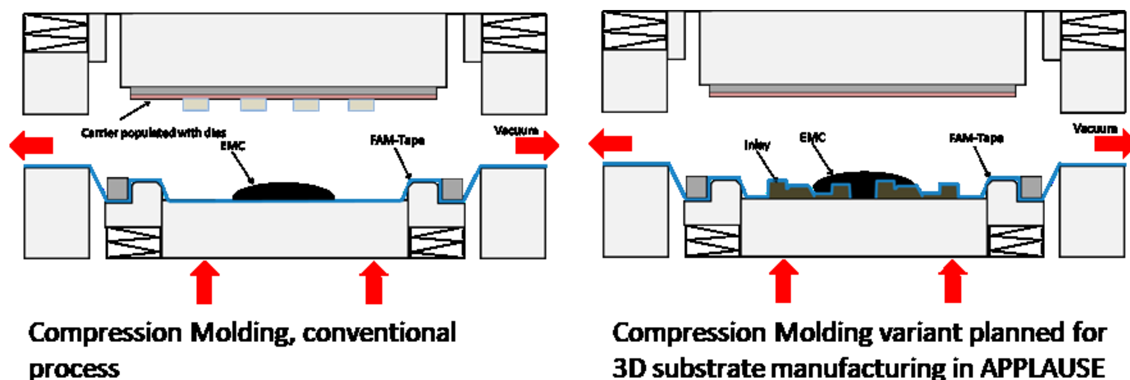


Figure 68: Sketch of conventional compression molding process (left) and modified approach for organic freeform substrate manufacturing (right)

Referring to the different parts of the sketch in Figure 68, various materials with impact on the accuracy of the resulting product were considered.

Basic orienting trials with different epoxy molding compounds (EMCs), varying in filler particle size, as well as in CTE and the amount of chemical shrinkage during crosslinking of the epoxy matrix were performed. Different FAM-tapes (Film Assisted Mold or Foil Assisted Molding) allowing for easy release of molded parts from the tool, were also investigated with a focus on determining the influence of thickness, compressibility, stiffness and roughness on the molding results. The inlay material, being critical for the overall outcome, was discussed with a focus on accuracy, thermal expansion and process cost minimization.

As for the 3D substrate in EMC the main factors to impact molding results are

- Molding temperature
- Molding pressure
- FAM type (material, roughness, thickness)
- EMC material (CTE, shrinkage)
- Inlay (CTE, geometry)

Furthermore, it must be mentioned that before the actual molding process begins, the FAM tape is sucked onto the bottom chuck (following the depictions above) and hence is drawn over the inlays, resulting in local strain and therefore potential thinning, at times even rupture of the tape.

In order to separate effects and to derive design rules for inlay manufacturing later on, we first relied on simplified inlay shapes. For this, simple inlays, accurately milled, were used with different process settings, various FAM tapes with different mechanical properties and thicknesses, as well as different molding pressures.

For tests, several mold wafers with different generic shapes were manufactured. Two examples of EMC-wafers with test-structures are shown in Figure 69. After molding experiments (at M12), 3D-analysis of the molded structures were performed. Results provided a better understanding of the molding process and the interdependencies of behaviour of the EMCs, FAM-Tapes and mold inlays as far as molded device geometrical precision is of concerns.

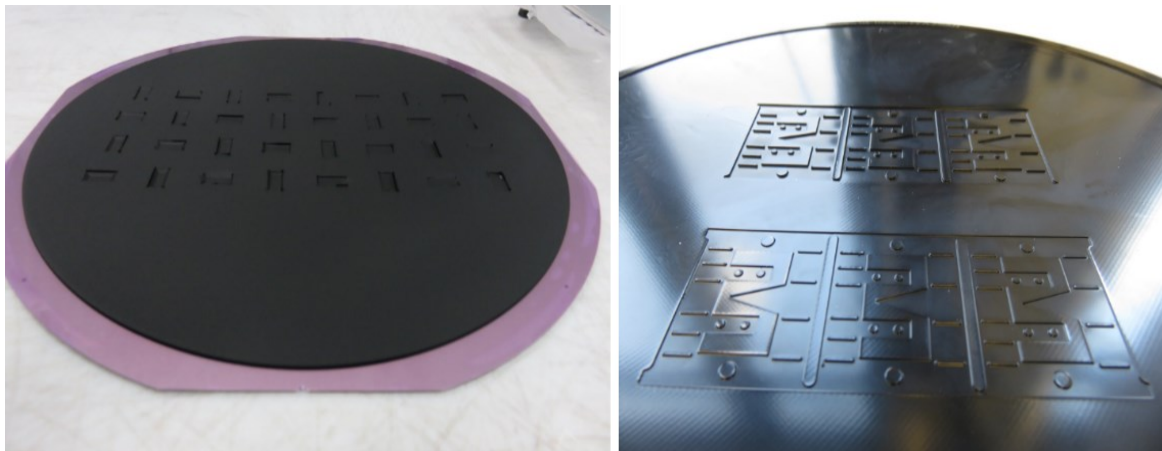


Figure 69: Test structures in EMC; first mold shot with mold inlays of varying heights and draft angles (left); mold shot with etched leadframe with different geometric shapes (right)

Task 4.5 b) Design and development of geometrical test vehicle

As a basis for following experiments, three different inlay types were manufactured and glued onto a 200 mm circular base in a 3x3 matrix with each inlay being present three times (Figure 70, a). The FAM tape being drawn onto the inlays by vacuum, providing a first shaping of the tape is shown in b) of the same image. The final shaping is then done under molding pressure during In Mold Cure (IMC) under process temperature (typically around 125 °C) and molding pressure (here, between 3.18 and 7.95 MPa). A top view of the final mold-wafer is depicted in Figure 70, d.

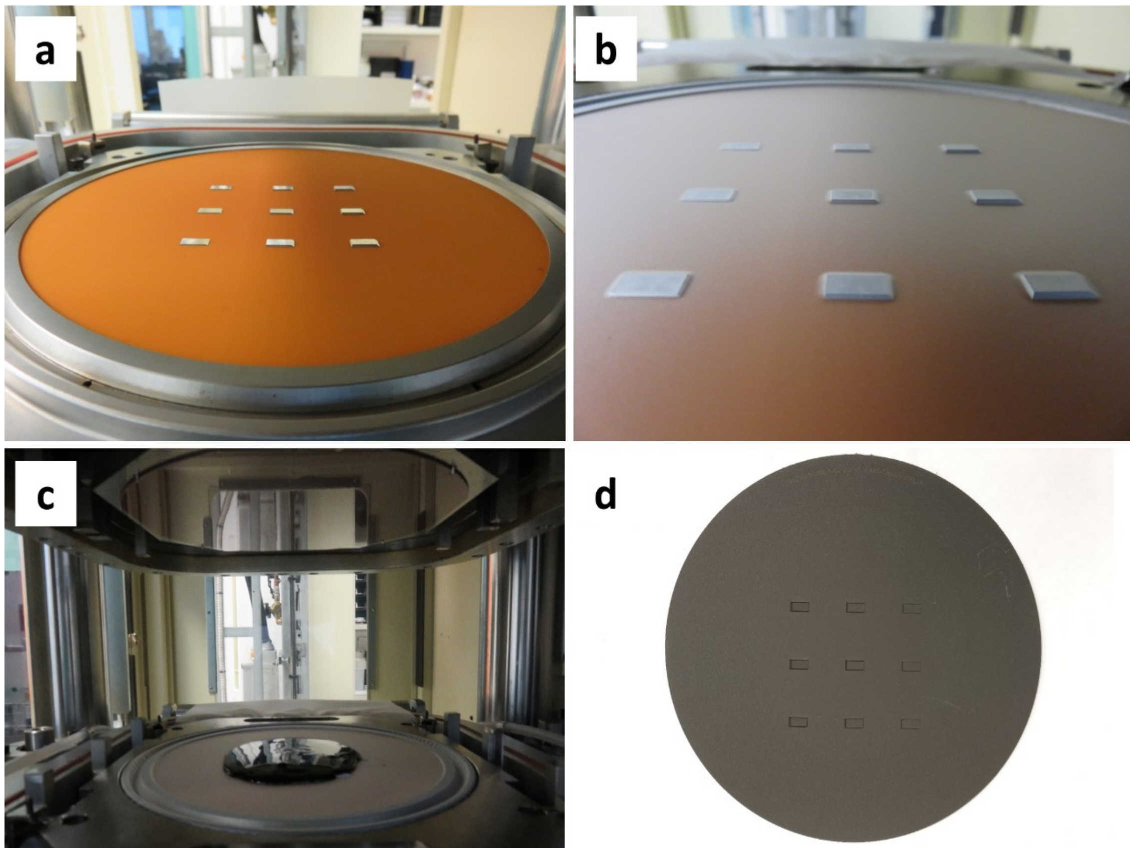


Figure 70: Molding process for inlays; a) inlay on base; b) FAM tape drawn over inlays (vacuum); c) EMC on FAM tape right before molding; d) view of formed cavities in EMC

A direct comparison of 3D scans of inlay and resulting cavity in the EMC can be seen in Figure 71 while Figure 72 shows the results of topography measurements after molding exemplarily, where the full set of results is providing the data on cavity depth after molding, FAM tape influence on mold cavity depth and the respective tolerances and also on the behavior of the FAM tape a the cavity edges. D4.7 summarizes the generated knowhow.

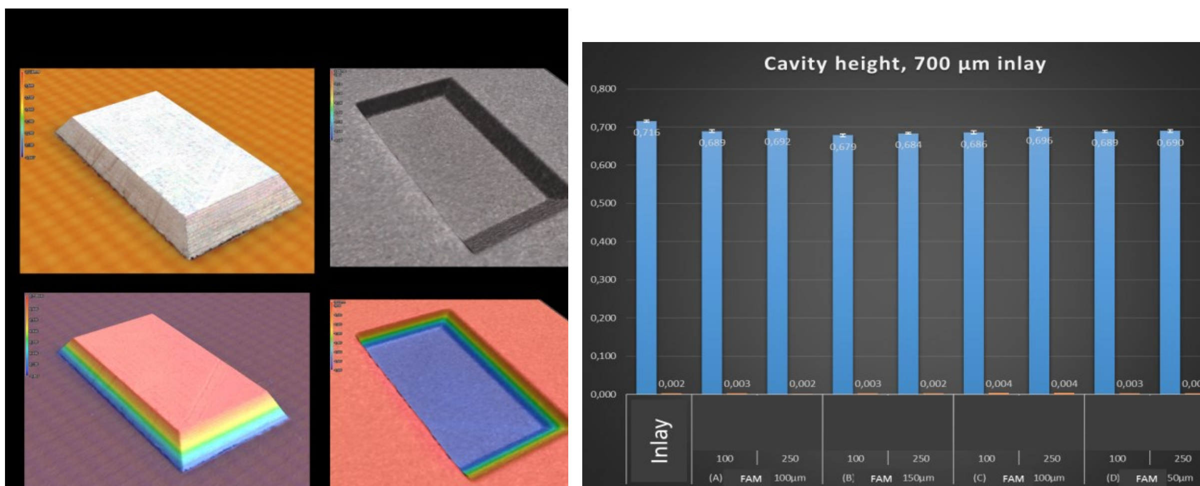


Figure 71: Exemplary results, 3D scans of inlay (left) and resulting geometry in EMC (right)

Figure 72: Cavity height measurements with varying FAM tape thickness and mold pressure (Std-Dev: ~2-4 µm)

The investigations described in D4.7 led to a generic comprehensive set of design rules on manufacturable cavities (3D freeform) into compression molded wafers, considering the FAM-tape (separating the molding compound from the inlays) behavior and the geometries of the templates. These design rules have been used to design a 3D template for the target 3D substrate of UC3. (see Task 5.3.1).

Task 4.3 c) Development of assembly process for integration of functional elements

In this task the 3D molding process is developed to create low-cost organic freeform submounts for optical assemblies. In communication with DustPhotonics (Use Case Leader), the spatial alignment of EML, lens element, isolator and fibre have been fixed and a first version of the package for Use Case 3 was designed and necessary premold (and thus inlay-) geometry was derived at M12.

Figure 73 shows the freeform substrate with components (isometric left and in cross-sectional view in the upper right), as well as the optical path (bottom right, provided by DPH). Using this as a starting point, the actual inlay geometry was developed. Manufacturability of the inlay, as well as smoothing influence of the FAM-tape (separating inlay from the resin during processing) and treatment of steps and corners of the inlays are considered.

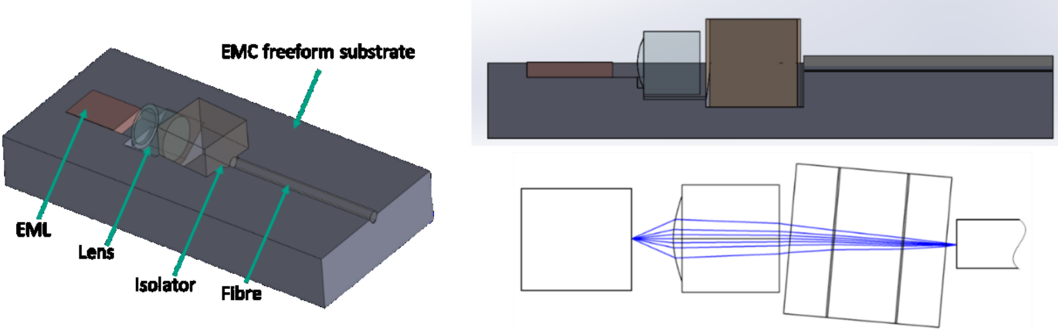


Figure 73: First package design featuring all components and spatial arrangement; Isometric view of premold package and assembled optical components (left); cross sectional view of assembly (top right); top view of optical path of the assembled system (bottom right)

Based on previous molding results with the geometrical inlays and derived design guidelines, the design of the milled steel inlay (Figure 74), which forms the basis of the submount for optical components (laser, lens, isolator and fibre), was finalized and the inlay was procured.

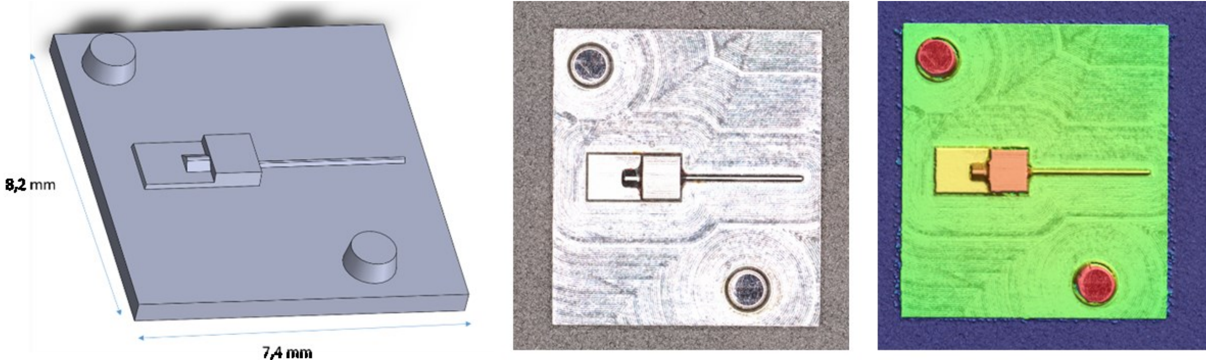


Figure 74: Milled inlay; CAD model (left), top view photograph (middle) and height image (right)

Using previously determined mold temperature, FAM-tape type (25 µm thickness) and adapted molding pressure to avoid rupture of the thin FAM tape, we were able to obtain promising

results. We note minor deviations with regards to the CAD model on the sidewalls. However, the size of the individual recesses and especially their height relative to each other is promising to allow for component placement well within the optical axis (Figure 75).

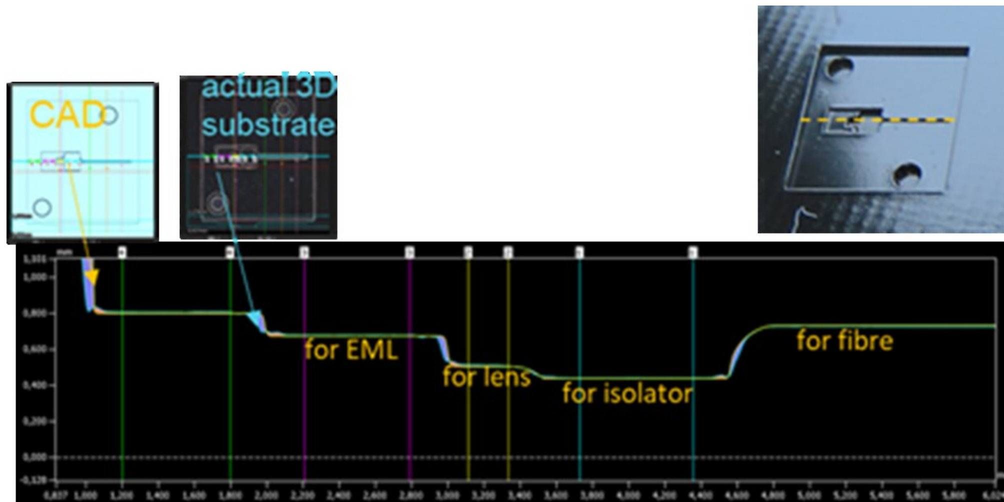


Figure 75: Comparison CAD model - molded substrate

Further work was done towards achieving complete fiducial sets for all recess depths. This was solved by trial iterations and first assembly trials were performed by Besi-AT on those 3D-Mold substrate. Exemplary results are depicted in Figure 76.

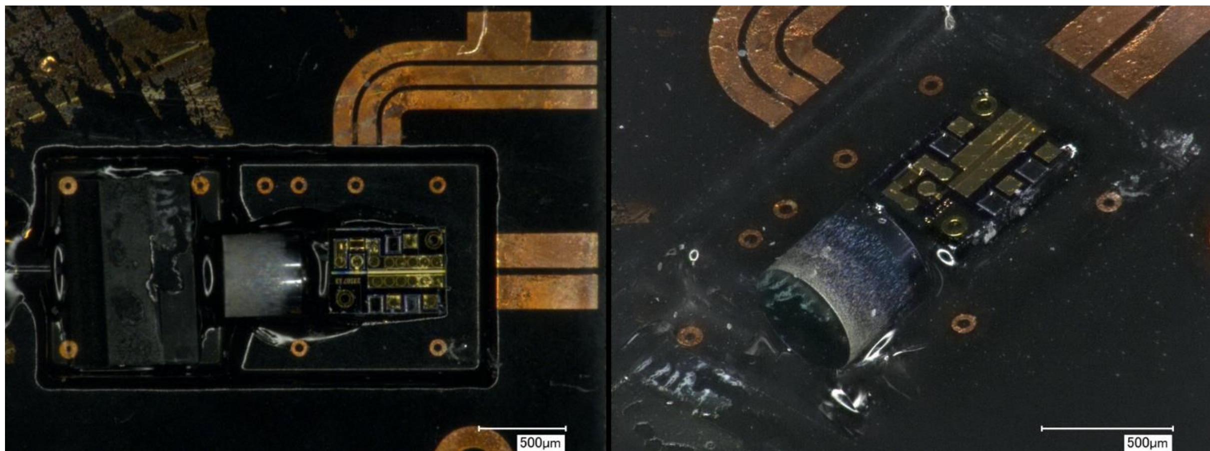


Figure 76: 3D molded submount after preliminary component assembly; top view (left), isometric view (right)

Component level fiducials, i.e. for the EML, lens, isolator, were complete. Corresponding 3D-Mold substrates were delivered to Besi-AT for high accuracy component P&P, which concludes work in WP4 and WP5. The Assembly strategies to ultimately allow for passive component alignment, as well as actual assembly are part of WP5 at the EU Partner BESI-AT.

Task 4.5 d) Process development for direct metallisation of mold coumpound

First steps towards a set of design rules for direct metallization have been considered. These include the treatment of height differences (steps), critical angles (e.g. steepness of sidewalls) to allow for successful demolding. On the other hand, as it is intended to realize direct Cu metallization, work towards requirements/design rules for signal routing and thermal management was started.

First RF-Simulations were conducted to properly lay out the conductors, considering tan(δ) and ϵ_r of the EMC. A close loop between the loss estimates from the simulations and manufacturability of respective Line/Space (L/S) on EMC was established. Figure 77 shows a preliminary conductor layout for Almae's EML. At this stage, wire bonding between pads and the EML die is foreseen, as the EML is die-attached / assembled face-up into the premold substrate.

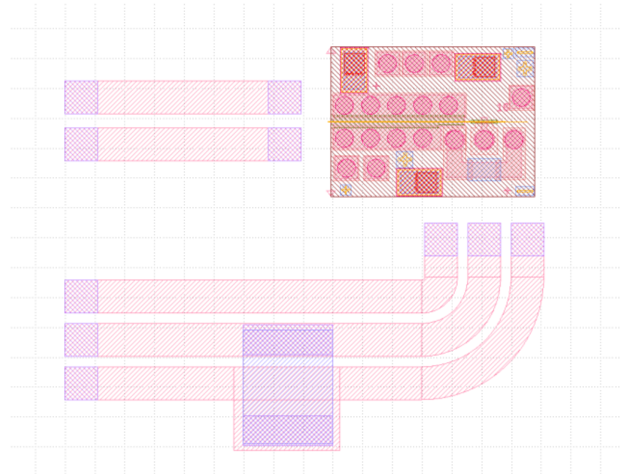


Figure 77: Preliminary conductor layout for lithography and etch tests

Then, we focused on realizing highly accurate component level fiducials at different heights (i.e. for the EML, lens, isolator, and fibre respectively). We adapted the process flow from subtractive to semi-additive to overcome processing obstacles related to plating and etching rates in the recesses, else resulting in incomplete fiducials. With semi-additive processing (Figure 78), Cu traces and package level fiducials are at different elevations and complete. However, we note missing fiducials in the deepest recess (yellow circle). Work to solve this was started within transfer to WP5. This improvement will then finalize WP4 work, and we will continue work in WP5 with the focus on assembly and integration.

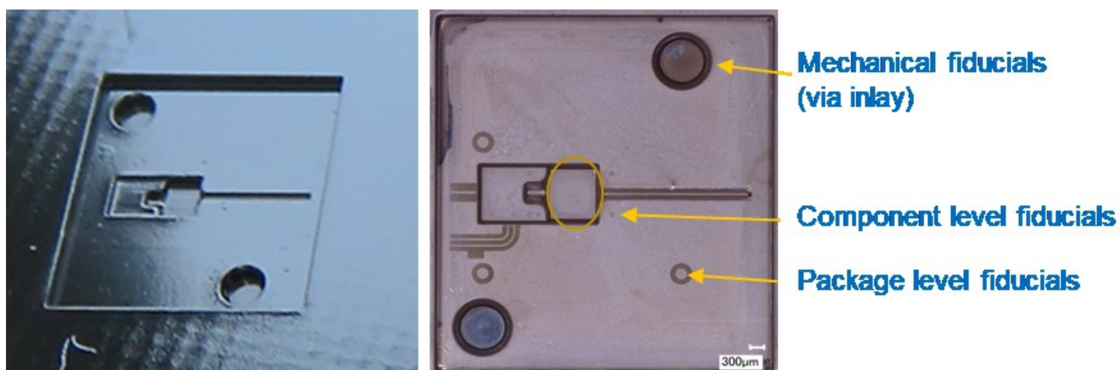


Figure 78: molded substrate; after molding (left), after subtractive photolithography (right)

The EU Report/Deliverable D4.7 - Geometrical precision of molded 3D substrates - gives further insight on the work performed.

WP5 Packaging and Integration

Task 5.2 UC2 packaging processes (Low cost thermal imaging systems)

The Task 5.2 was completed during the reporting period 2022. All parts for hermetical sealing were prepared, as described in Figure 79.

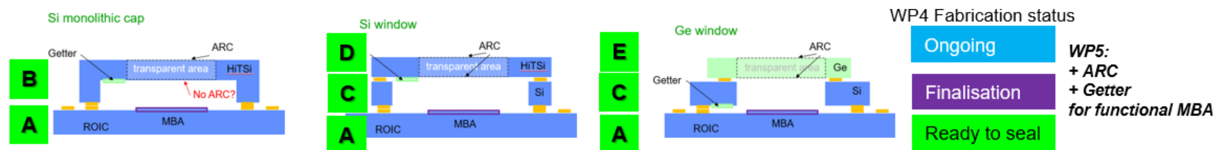


Figure 79: Status wafer preparation

A conference paper recapitulating the performed work in T4 and T5 was presented at ECTC 2023: Kai Zoschke et Al., Wafer Level Capping Technology for Vacuum Packaging of Microbolometers, ECTC2023 Orlando.

Task 5.2.1 Cap wafer

On the side of the antireflective coating and its integration in cap, evaluation tests (Figure 80) with most critical wafer bonding processes have been performed on “dry-runs” and the coated samples analysed in IR-transmission and reflectivity (Spectra LWIR, not shown). It permits to define at which point the ARC can be integrated, which wafer bonding can be tolerate without dramatic damage of the ARC properties, and to trigger the entire wafer process flow.

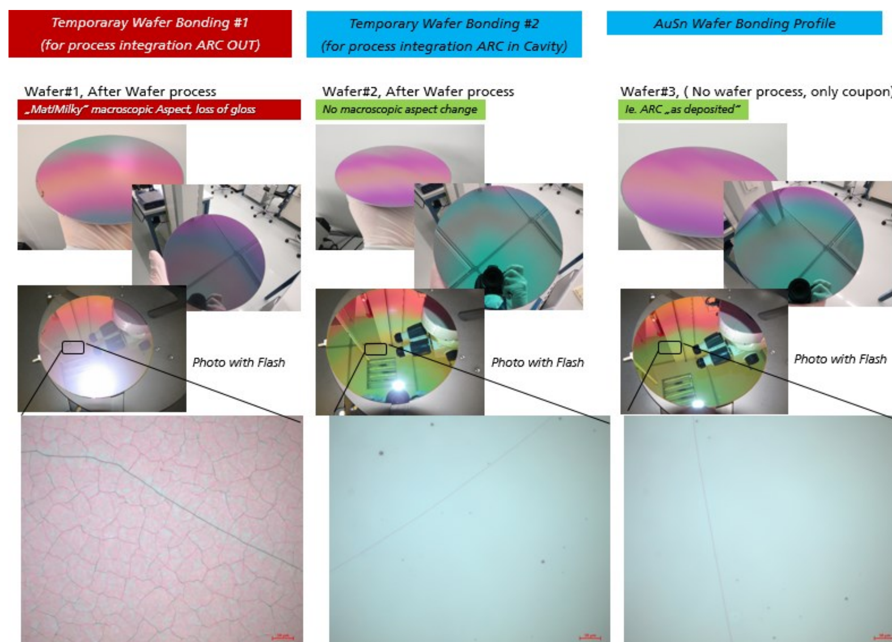


Figure 80: wafer level evaluation tests of Antireflective coating (semi-commercial product)

Based on results of WP4, silicon monolithic Cap wafers were finalized (Figure 81) and included an Anti-Reflective coating deposited on the later outer side of the cap. After cavity etching, a getter material has been also successfully deposited on the inner side of the caps (subcontracted), on top and/or bottom of cavity (design variations) prior bonding to base/device wafer.

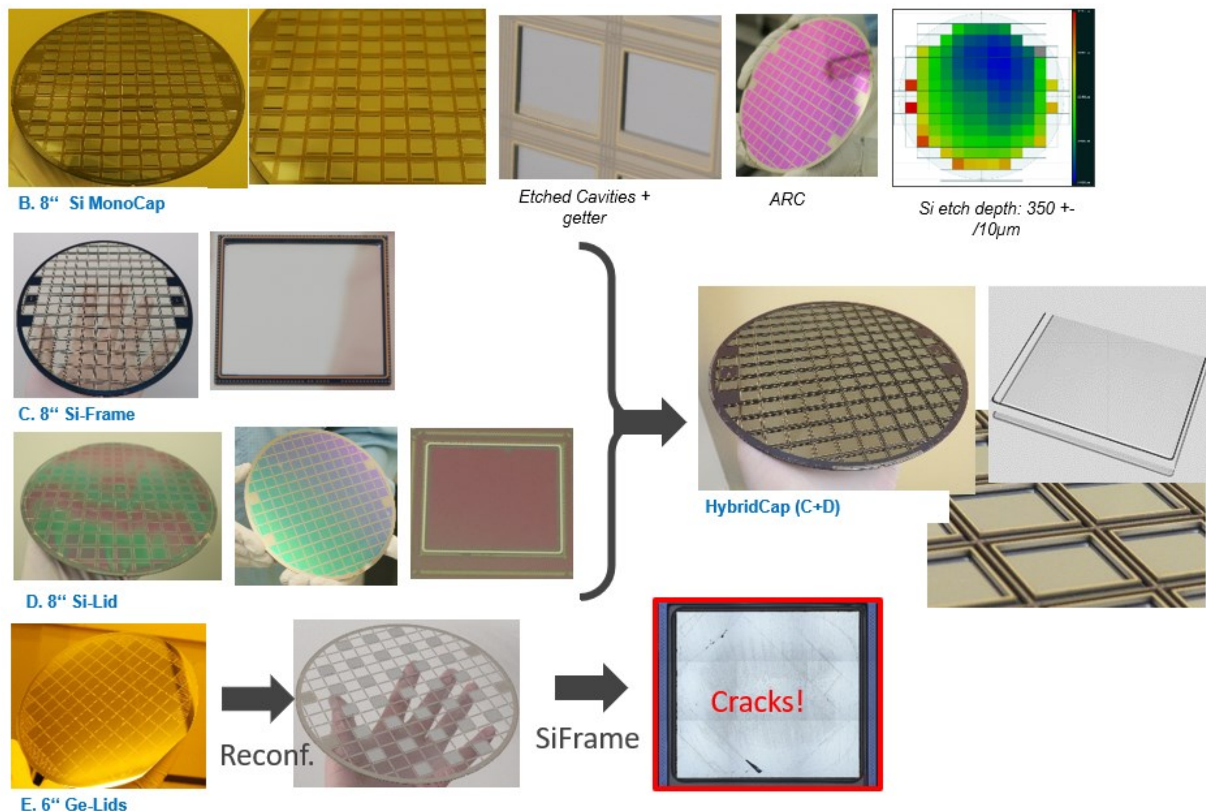


Figure 81: different cap wafers (silicon monolithic cap wafer is on top, example)

Task 5.2.2 Preparation of microbolometer for WLP

Compatibility of MBA+ROIC wafers with flat from IDEAS (JEIDA Wafer) on the machine park has been evaluated, resulting in the need of special fixtures for wafer handling, especially for electroplating / semi-additive deposition of the sealing ring on MBA+ROIC wafers (ring contacting of the plater electrodes on the wafer outer ring).

Two wafer types were successfully prepared:

I. Microbolometer wafer materials from IDEAS/NNFC
II. Pirani Sensor from Fraunhofer IMS

For the microbolometer of IDEAS (i), tests for protecting MEMS Bolometers during back-end processing at IZM have been done as well as the release of the protecting overcoat (WP4 also). Those tests permitted to verify the compatibility of the overcoat processing, especially to deposit the AuSn bond rings around the MEMS arrays by electroplating without plating and damaging the thin MEMS membranes (Figure 82, Figure 83 and Figure 84). Light microscopy supported by SEM observations assessed the process feasibility without deteriorating the MEMS integrity (no functional cross-check tests, only visual analysis/inspection, since no functional devices were available).

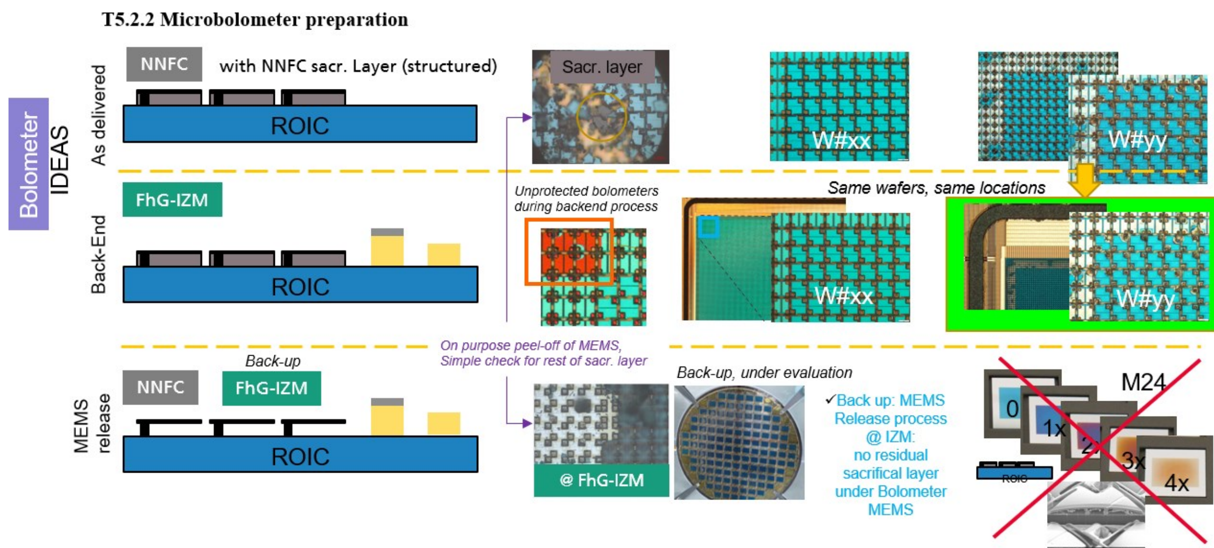


Figure 82: overview of work on preparation of microbolometer for WLP (IDEAS/NNFC Bolometer MEMS), with overcoat protection and removal during WLP.

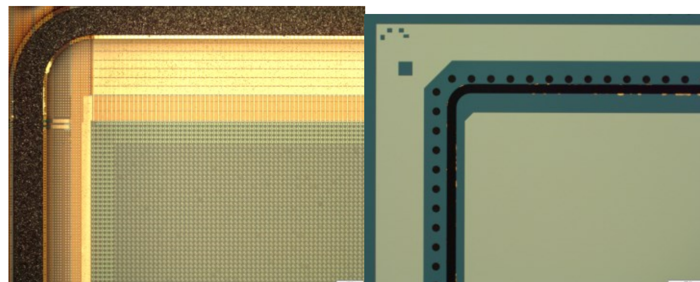


Figure 83: left: AuSn bond ring on IDEAS/NNFC device bolometer (non functional) ; right: FhG-IMS dummy wafer (ring in open area of structured MEMS IMS sacrificial layer only)

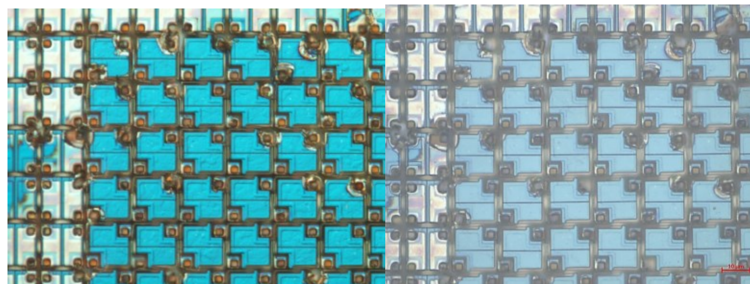
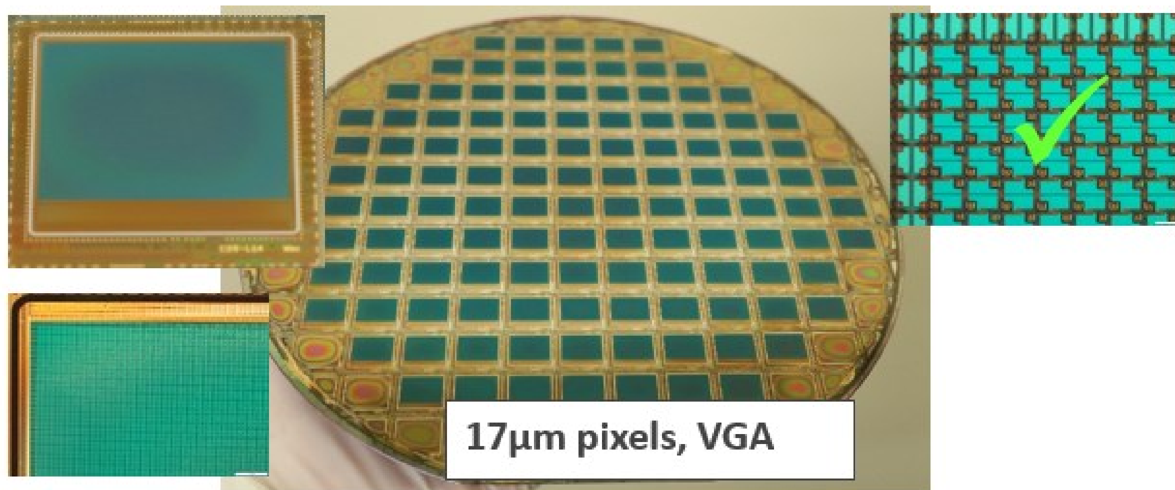


Figure 84: left: IDEAS NNFC Bolometer (non functional) as received (wafer center) ; right: after overcoat protection, AuSn Bond Ring deposition, overcoat removal and removal of NNFC amorphous carbon release Layer (MEMS support layer) at FhG-IZM. Nota: not same microscope.

Finally, the processes tested in WP4 and used at Fraunhofer IZM for preparing the base/devices did not damaged the MEMS structures, in both cases (IDEAS Microbolometers and FhG-IMS Piranis), and were compatible with the MEMS release processes, i.e. when the support material (released sacrificial layer) whereon the thin MEMS membranes are fabricated is removed (Figure 85).

Nevertheless, no functional microbolometer wafers were made available from the project partner IDEAS. In consequence, the T5 works focused mostly on the version of pirani sensor, especially bonding/hermetical sealing with monolithic cap wafers. This aimed to advantageously use the prepared best cap wafers to investigate the vacuum enclosed in the package.



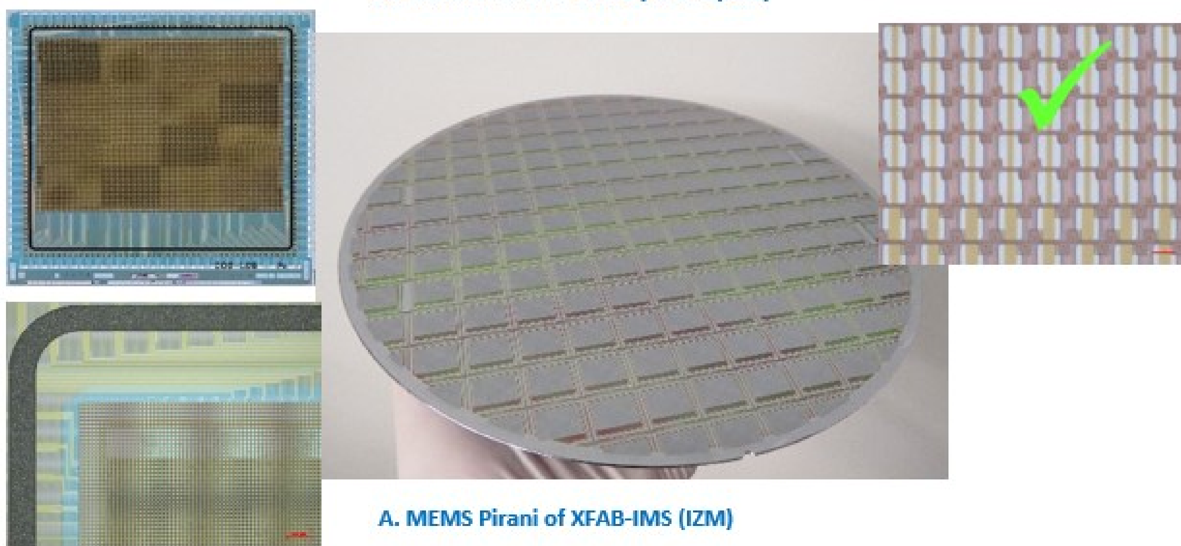


Figure 85:prepared base/device wafer, Microbolometer shortloop (top) and passive MEMS functional pirani sensor (bottom) after release of the respective sacrificial layer.

Task 5.2.3 Hermetical Encapsulation

Using the results of task 4.2, the hermetical bonding could be performed (Figure 86) up to a yield of around 99%, inclusive device singulation, with the MEMS Pirani sensor, as estimated by the deflection in the silicon cap (Figure 87).

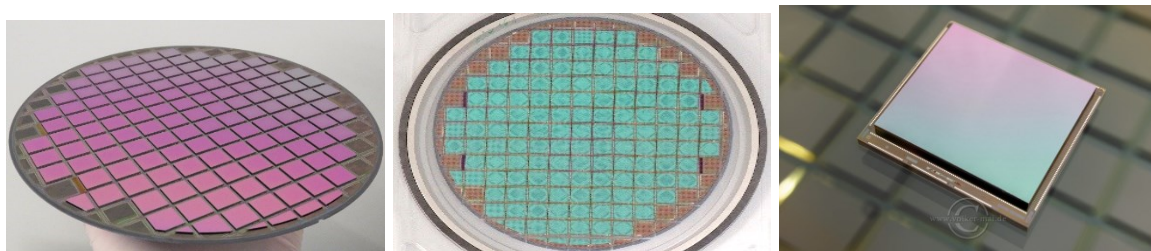


Figure 86: Pirani MEMS Wafer bonded with monolithic silicon cap incl. getter and anti-reflective coating (left), and after device wafer dicing (center & right)

Further attempts of bonding hybrid caps onto MEMS Pirani Wafers were undertaken, in order to compare the cap topologies in regards of vacuum enclosed inside the package, ie. comparison between monolithic and hybrid caps, and the effect of the getter. However, the results with the hybrid caps were unsatisfying, with low wafer yield, due to poor AuSn wafer bonding quality between Si-lid and Si-frame wafer by forming/assembling the hybrid cap. The first reason is due to some misalignment between lid and SiFrame during the wafer bond sequence. The second one (as mentioned in T4) is a process issue as revealed by SEM and EDX analysis (WP6), more present on some wafers, during bond ring fabrication affecting the adhesion of the metal bond rings to the bulk and leading to random/poor results.

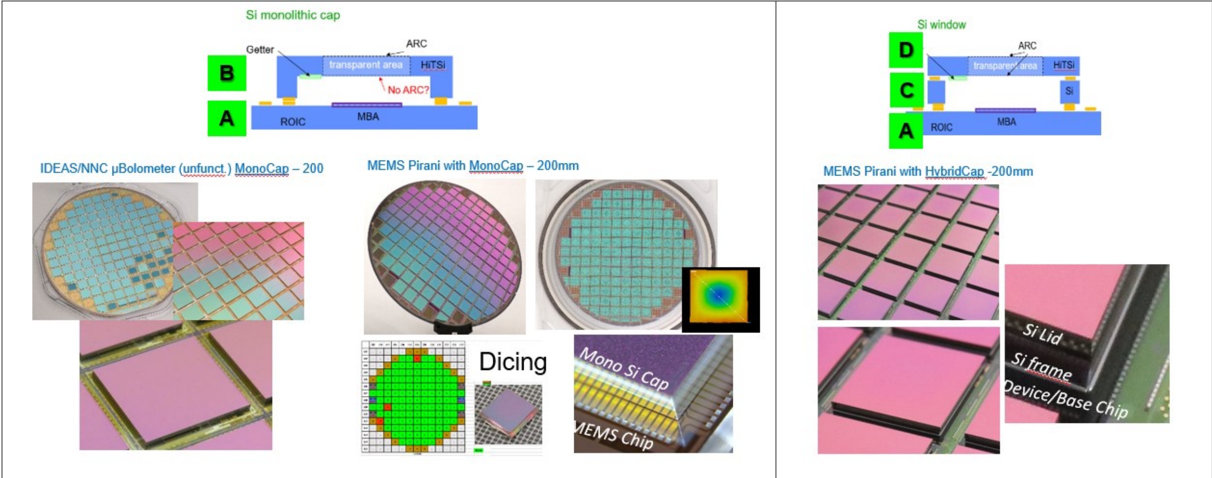


Figure 87: AuSn Wafer Level Vacuum Hermetic Bonding, with monolithic cap on IDEAS and Pirani Wafer (left) and hybridcap on Pirani (right), examples.

The IDEAS short loop wafers presented also some problems in the bonded rings. Top Oxide Passivation (device wafer surface) on those delivered unfunctional device wafer was far too thin (~20 nm), as already identified at project start by FhG-IZM and communicated to IDEAS, leading to reaction of the gold-tin solder with the Si-bulk (AuSn-Si reaction).

Cap corner		Cap edge	
a. Focus Seal Interface	b. Focus MEMS Microbolometer	a. Focus Seal Interface	b. Focus MEMS Microbolometer
Seal Ring	Microbolometer array	Seal Ring	Microbolometer array

Figure 88: Inspection of sealed Microbolometer with Infrared Microscopy through polished Si Cap

After wafer bonding, the wafer stacks were inspected visually, deflection of silicon cap measured, the bonded ring were inspected by X-Ray and IR photography, IR microscopy (Figure 88), CSAM, etc (WP6). After singulation, the devices were inspected destructively per cross-section and the bonded rings inspected by light microscopy and SEM/EDX (metallurgy, layer stacks, delamination if any). Figure 89 presents also examples of cross-sections of the packages with hybrid cap and monolithic cap and of the bonded rings.

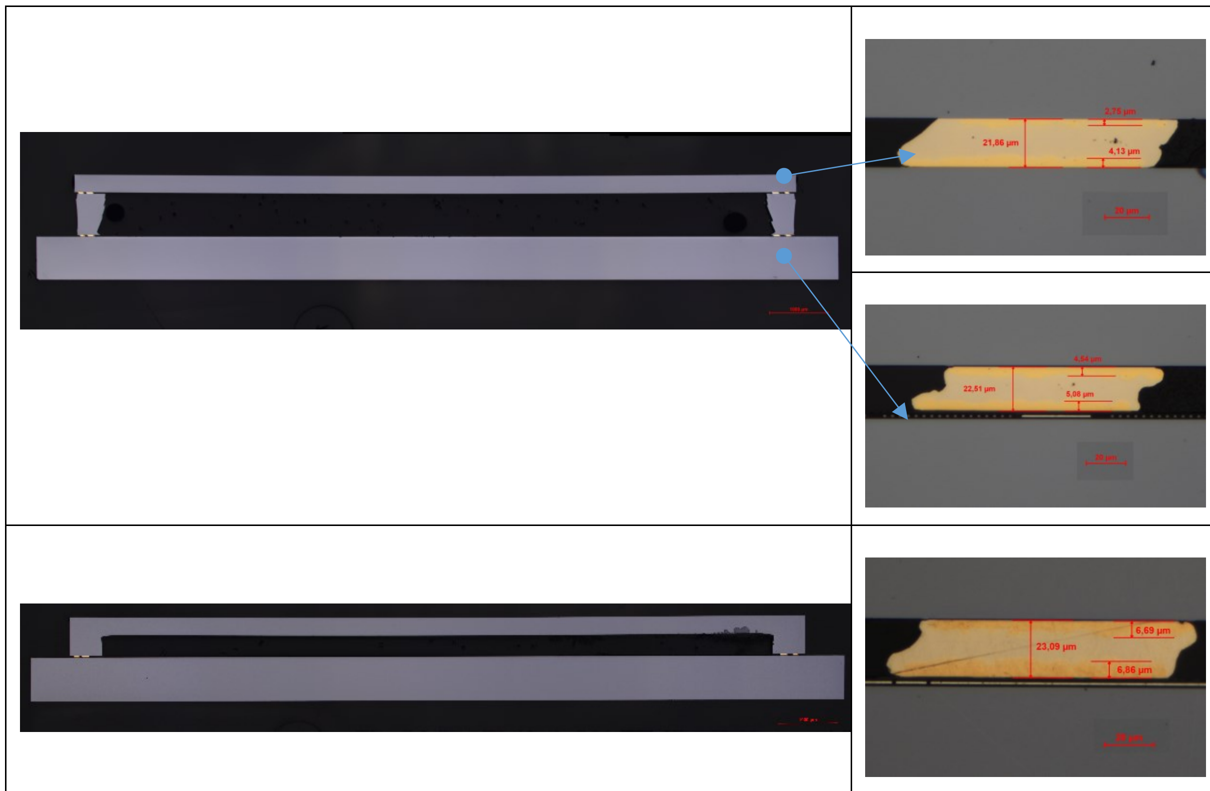


Figure 89: Cross-sections (examples) of capped pirani devices and bonded AuSn sealing rings: hybrid cap (top) and monolithic cap (bottom). Device is ca. 13.6 mm long, cap length ca. 12.3 mm

After singulation of capped wafers, singulated capped die were dispatch among project partners. Amongst other, Pirani MEMS were measured in a tentative to assess the vacuum level inside the diced devices. Partner USN (Norway), in charge of MEMS Pirani design, characterized the Pirani MEMS of bare/uncapped device chips from IMS (MEMS Fabrication), originating from the same MEMS Wafer batch, in a vacuum chamber to extract a reference/master/calibration curve (MEMS resistance vs. pressure), however in a limited range of 0.1 to 10 mbar, due to equipment constraints (Figure 90, left) .

In parallel, within task 6.2, Fraunhofer IZM undertook with wafer probing the resistance measurements of all pirani designs (2x6, ie. on top and bottom of die) on singulated capped chips, from wafer center and edge, inclusive different cap designs (Max, G+, Px, cavity size variation and/or getter area) . The most sensitive MEMS design was found to be “Pirani_11”, corresponding results are presented in Figure 90, right.

A vacuum of 0.1 mbar could be assessed, or even lower (resitance value out of lower range of master curve). Some gradient can be noticed between center and edge of wafer, probably due to degassing during wafer bonding. Getter definitally ameliorates the vacuum quality.

Further tests were performed with post bond thermal annealing, to further activate the getter, first results show a further drop of the pirani resistance ie. amelioration of enclosed vacuum (see WP6).

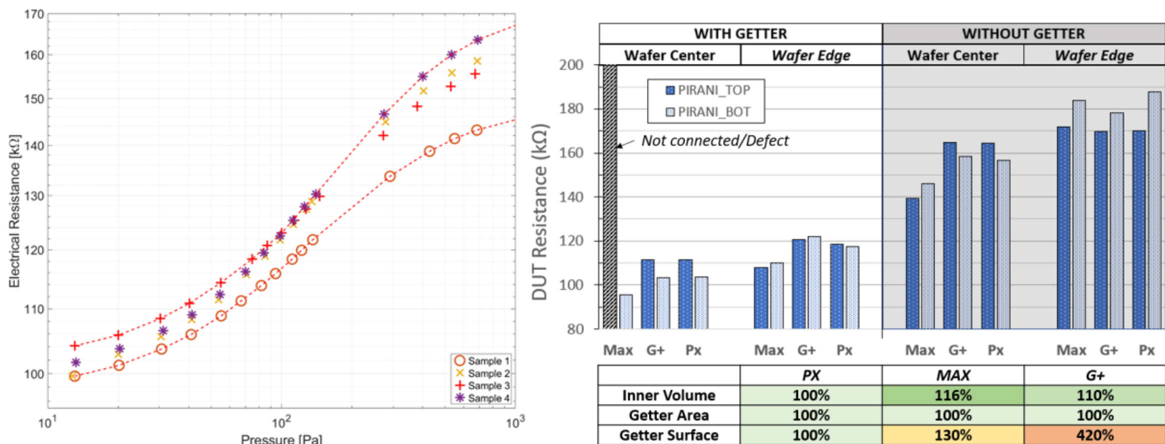


Figure 90: Calibration curve of "Pirani_11" (Source: USN, Norway) and measured electrical resistance of it (diced chips) @ FhG-IZM with wafer prober

All tasks were finished according work flow plan (Figure 91) to perform the wafer level packaging of MEMS-based microbolometer sensors, in two different MEMS fabrications (MEMS Microbolometers from IDEAS, MEMS Pirani from FhG-IMS).

Results were presented at ECTC 2023, Orlando, USA in the paper of Kai Zoschke et Al., Wafer Level Capping Technology for Vacuum Packaging of Microbolometers, ECTC2023 Orlando

The EU Report/Deliverable D5.2- Report on packaged microbolometer - gives further insight on the work performed.

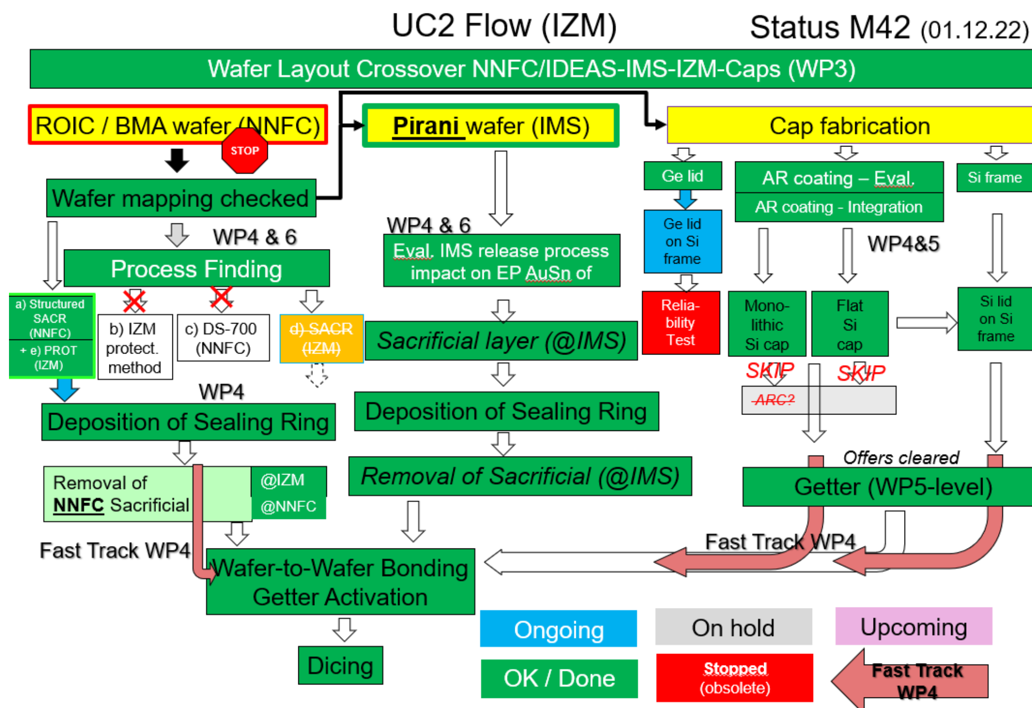


Figure 91: Status of Work flow within UC2 (WP4 & WP5)

Task 5.3 UC3 packaging processes (Passive fibre alignment for single mode transceivers)

Task 5.3.1 Development of a 3D-mold and metallised substrate suitable for UC3

T4.5 and T5.3.1 are strongly linked. T4.5 focuses on the 3D freeform molding process and subsequent conformal direct metallization on the epoxy molding compound (EMC) whereas T5.3.1 targets more use case (UC3) specific topics, such as component placement, related assembly strategies and correlated adhesive materials and their processing. First submount samples were provided to and for Besi-AT for assembly, without full fiducials. Target was to establish an assembly process to overcome height variations of the EML die itself (TTV of InP laser wafer from grinding), which result in a random vertical shift of the optical axis. Also, manufacturing-process related slight shifting of the v-groove is considered.

Within this task, it has been demonstrated that a 3D freeform molding is possible and that no fundamental geometrical limitations do apply for the target geometry of UC3. Nevertheless, the precision necessary to manufacture a functional demonstrator based on molding processes is not reached yet and needs additional research. The basis for a first UC3-compatible 3D substrate has been reached, design rules for molded 3D substrates and for directly metallized structures have been generated and a reference design for a molded 3D substrate has been developed (see Figure 92 and Figure 93), also based on process development in T4.5 within WP4. This substrate aims for research on component and system integration, the possibility to create conformal conductors along angles surfaces has been explored. This will serve to eliminate wirebonding from the assembly and integration process, as well as allow for component placement into cavities in a face down flip-chip manner.

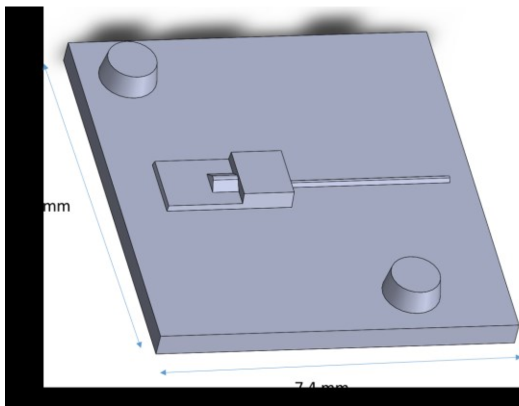


Figure 92: Sketch of a 3D inlay for molding a UC3 demonstrator substrate based on D4.7 design rules

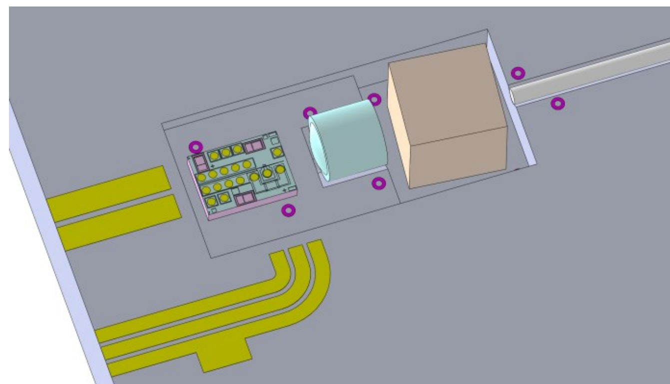


Figure 93: Sketch of a 3D substrate with metallization, fiducials and components based on molding technology

A milled steel inlay based on the designs introduced above was procured and used for manufacturing of molded substrates. Also metallization processes for these 3D substrates were investigated and subsequently assembly trials in T5.3.2 performed at BESI-AT.

Precise cavities for the EML and Isolators were formed alongside with V-Grooves for the µLens and Fibre. By means of Semi-Additive Plating (SAP), DC-power supply and HF-signal-lines and package level fiducials were formed on the mold topside (Figure 94, top right). Component level fiducials on their respective z-levels, to allow for high accuracy bonding in accordance with Besi Systems – also being developed within APPLAUSE, have been also generated in the same step.

Organic submounts were delivered on time for WP5 grade assembly at BESI-AT (Figure 94, bottom), which should have performed the assembly within an allocated machine time. One of the specificities is the potential for scaling, i.e. by forming a large number of such 3D submounts in one molding step. Development of this work was done on 200mm wafer formats but is in principle scalable up to larger (panel) form factors of up to 610 mm x 457 mm (24” x 18”).

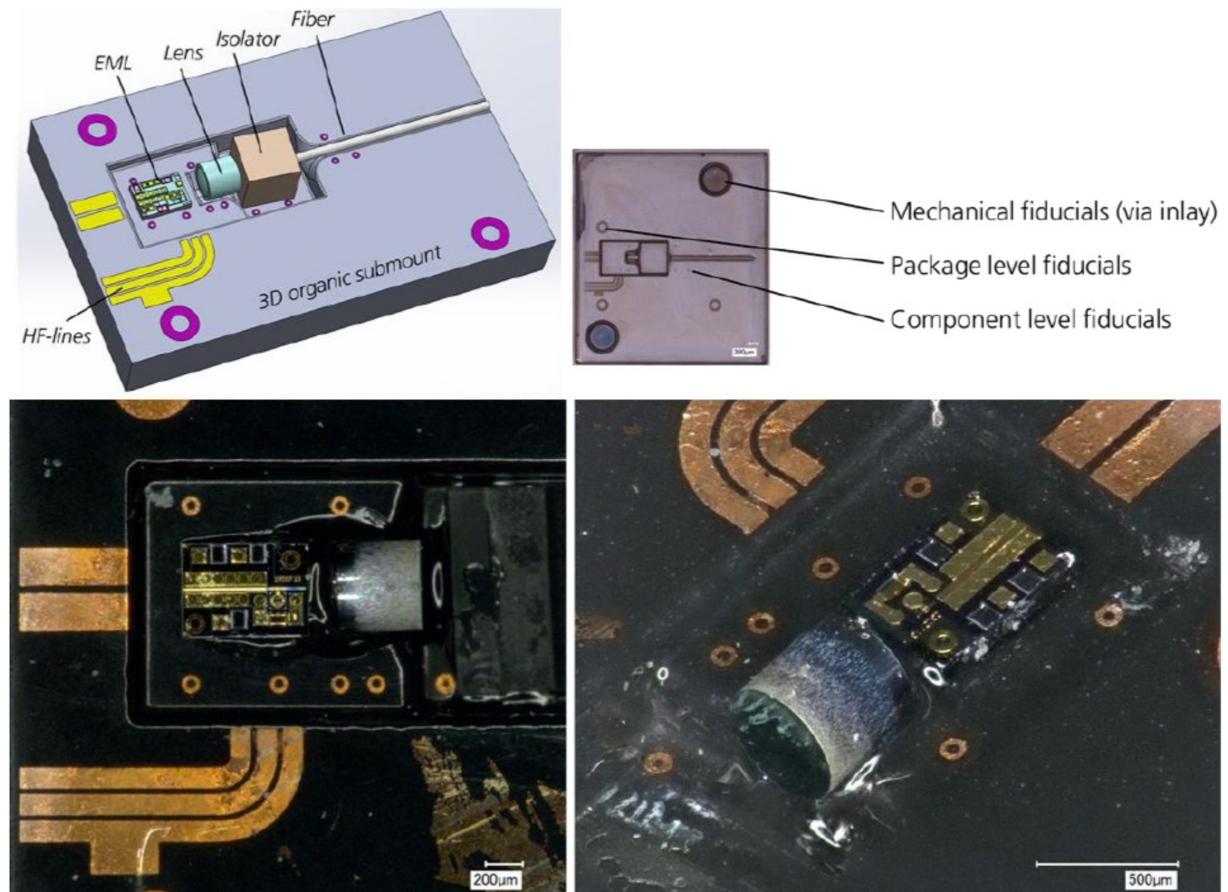


Figure 94: Package Sketch UC3 based on 3D organic submount and test assembly at BESI-AT

Task 5.3.2 3D assembly process (3D Silicon Bench)

Due to increasing technological challenges generated by 3D topography along the 3D Silicon bench fabrication, work was parallelized between WP4 and WP5. Most of the work had to be in priority concentrated on WP4, to enable a first version of the silicon bench for assembly trials (with also first parts of first generation distributed to BESI-AT in Apr.22).

A. Fabrication of 3D Silicon bench substrates

The fabrication can be briefly summarized as follows. Fabrication starts with a 200 mm blank silicon wafer. The silicon is first structured with a Vernier near the outer edge of the wafer by means of silicon wet etching technics to reveal the <111> crystal plane orientation and the (100) surface orientation, which actually defines the general optical axis of the 3D Silicon optical Bench (fiber v-grooves)

Then the bulk is structured/micromachined from its original top surface using a combination of silicon dry etching and wet etching processes. The mask for the fiber v-groove is specifically

aligned onto the wet-etched Vernier presenting the best etched pattern, in a dedicated manner for each single wafer, since surface orientation slightly varies from wafer to wafer.

After the entire Silicon structuring, wherein flip chip 3D stoppers (~ -4 µm) are fabricated by dry etching as well as flip chip recess (~ -31 µm) and cavity-recess for the later mounting of the isolator and the light path opened, the wafers are metallized for HF routing with a 3µm thick electroplated gold layer and then with flip chip bumps of adequate height for mounting the EML using semi-additive processes. Two different types of bumps are fabricated by electroplating, Au bumps for flip chip thermocompression bonding and AuSn bumps for flip chip solder self-alignment. Due to the unusual very high and irregular surface topography, all additive and subtractive processes are performed using spray or combination of spin and spray lithography and proximity exposures (due to photoresist climbs on top surfaces induced by their surface tension). Figure 95 gives a brief insight of the evolution of the silicon over the entire fabrication process.

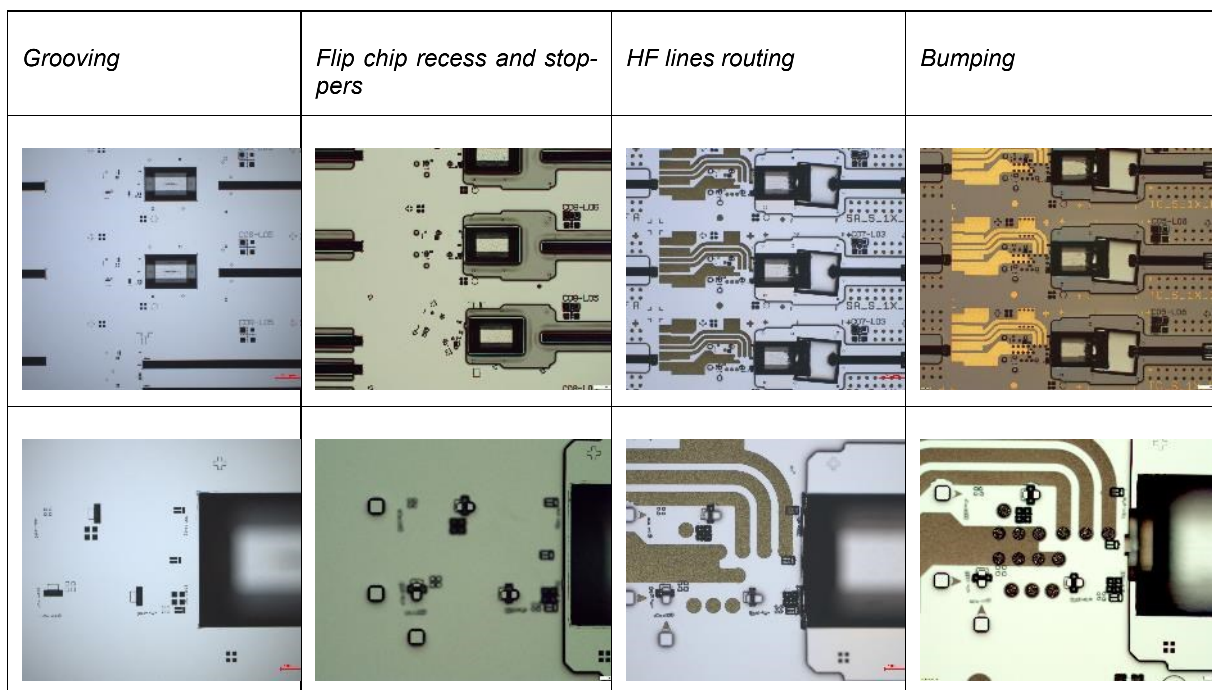


Figure 95: Wafer level Fabrication overview of the 3D Silicon Optical Bench

During the entire fabrication, wafers must have been secured onto temporary carriers, the deep silicon structuring weakening the wafers and leading to repetitive wafer break and cumulating wafer loss (Figure 96).

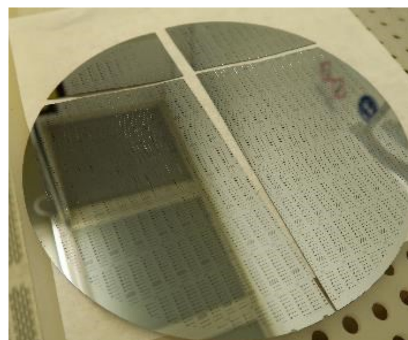


Figure 96: Example of Wafer break during rinsing

B. Flip-Chip Assembly

Flip chip thermocompression assembly trials (Figure 101) were performed, with the high precision flip chip bonder at Fraunhofer IZM, to connect functional laser chips onto the 3D HR silicon optical bench. In order to parallelize optic assembly work, lens and isolators were procured to FhG-IZM from BESI-AT, to test the optic assembly, perform metrology of assembled parts (Figure 121) and identify possible issues for optic assembly at BESI-AT (taking over the free space optic mount due to withdraw of DPH) and possibly assembled a transmit sub-element, in the frame of available resources and equipment's (originally optic mount not planned/no task at FhG-IZM). In-between, first isolators of BESI-AT were not fitting the planed dimensions and new isolators had to be late procured by BESI-AT (Oct.22).

To proceed with the considered FC TC process with use of z-stoppers, the fabricated 3D silicon benchs are first required. Figure 97 gives an overview of the FC bonding area, including the metal layer for IO routing inclusive the GSG lines for the modulator of the EML chip, the vertical silicon stoppers ("z-stoppers") and the electroplated gold micro-bumps, the markers and a typical 3D profilometry inspection.

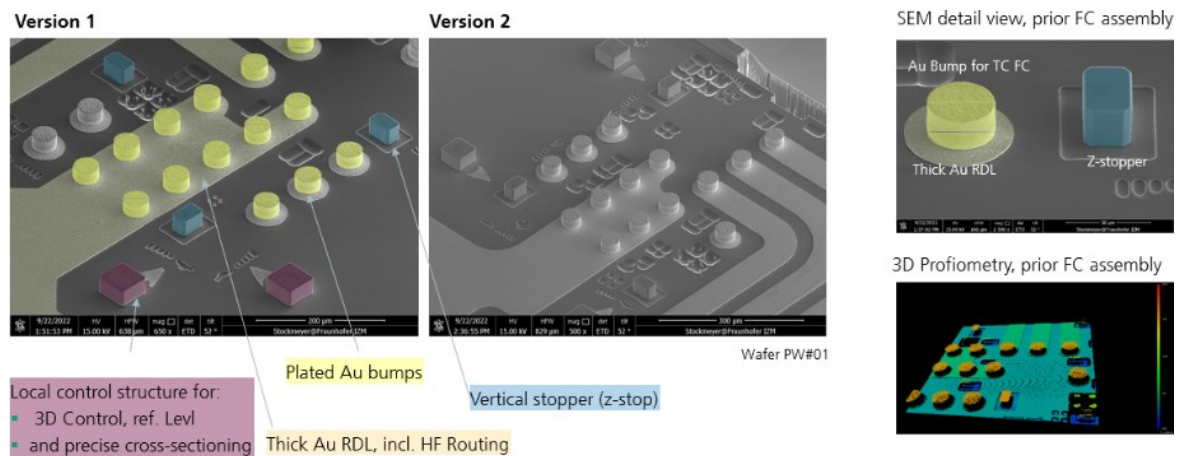


Figure 97: 3D Silicon bench for flip-chip thermocompression with Au bumps and stoppers (1st substrate generation)

EML chips were first mounted on 3D silicon benchs (of 1st generation) with Au bumps with the precise FC bonder. The correct alignment was checked with the control marker of the substrate and the waveguide of the EML:

a. Pre-bond: using the vision system of the bonder after the alignment sequence
b. Postbond: using infrared microscopy from the polished Silicon backside of the Silicon submount as shown in Figure 98 (through submount, since the EML chip being metallised on its backside, hindering infrared microscopy)

It can be also noticed that a postbond inspection using infrared inspection of superpositioned marks cannot be effectively performed: due to the fabrication of flip chip recess, the "photonic" (ie. absolute marks created with the V-Groove of Fiber) marks etched in Silicon appear too dark and are not transparent enough due to:

- Their surface roughness
- shape coarsening during the etching of the flip chip recess
- and infrared microscopy resolution.

This double control (pre and post bond) is probably not precise enough in regards of the target application (postbond precision < 1µm) but permits at least a rough pre-evaluation of the alignment, prior mounting any free space optics (lens, isolator, fiber) for optical testing. Effectively the required alignment for final correct operation cannot be basically and easily controlled using traditional non-destructive methods without (i.e before) assembling the entire optics. The only meaningful control remains in the end the mounting of all optic elements inclusive the fiber and test the entirely assembled system, representing a major drawback of the passive alignment.

As such, PostBond metrology is an important aspect especially in the case of passive alignment (and represents another challenge in itself), especially in the case of flip chip combined to 3D and submicrometric targets.

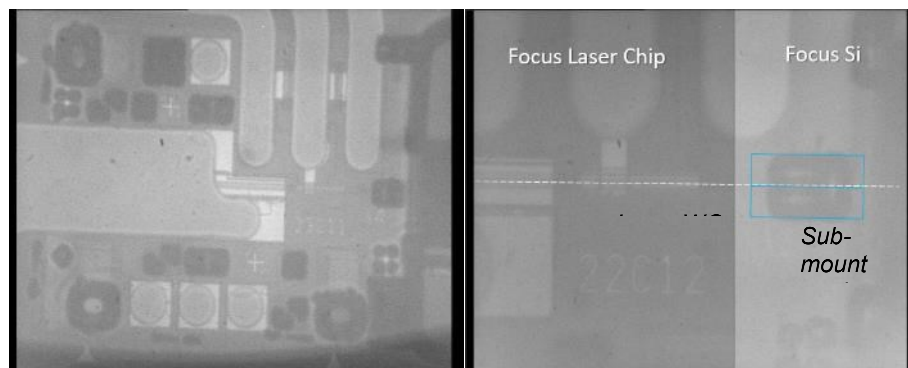


Figure 98: FC TC postbond infrared inspection through polished backside of silicon of 3D-Submount (EMLv2). The EML waveguide appears to be well aligned to the submount marker materializing the X/Y position of the 3D Si bench optical axis

In the scope of mounting an entire TX sub-element (ie. the optic parts, activity of BESI-AT), thermocompression experiments were performed at Fraunhofer IZM in “over-regime”, to make use of the mechanical stoppers and surely mount the laser chip, i.e. with higher bond forces than necessary to sufficiently deform the Au bumps for bringing surely the FC EML on their mechanical z-stoppers. Effectively, the stoppers are not only here to position the chip on the optical axis but also to ease the precise flip chip by stopping the FC thermocompression bond process in an effective, robust and repeatable way, without “particular care” on the final/maximal bonding force (and bonder speed).

Within these experiments, no crack could be revealed in the InP chips, neither from the stereomicroscope and infrared observations nor X-Ray, which first led to the conclusion of a correct mount of the flip chip laser. However, it appeared in cross-section analyses, that the laser chip was indeed sitting on the vertical stoppers, the gold bumps correctly compressed, but the laser chip not correctly connected to the deformed gold bumps. A fine gap could be distinguished between the bumps and the IOs of the laser. An example is given in Figure 99 for bumps (mechanical, not electrical) lying in the same plane of the stoppers.

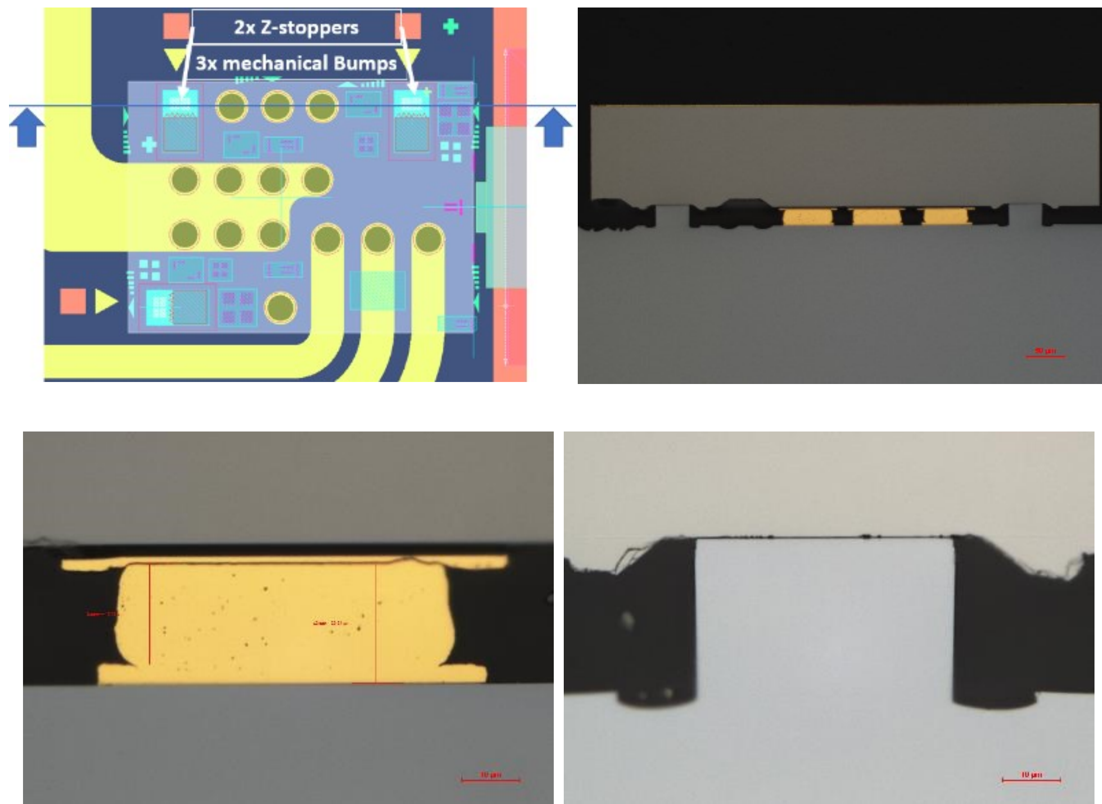


Figure 99: Flip chip thermocompression in over-regime, cross-section inspections.

The monitoring files of the FC bonder were further precisely examined, especially in terms of displacement and force, for both EML chip types, in order to understand and possibly identify any root cause. The traces of the force vs. the displacement of the flip chip bond arm (Figure 100, Left) do reveal several domains with different slopes. It is supposed, that the different slopes reflect different compression regimes

- the elastic compression followed by the plastic deformation of gold bumps (green domain),
- then entering a softer domain where the bumps further deform (orange area), possibly with some bump barelling,
- before coming into contact to the mechanical vertical stopper, where the slope suddenly gets steeper (red domain), probably due to an elastic mix-deformation of the bonder parts (arm and chuck) and the assembly (the silicon of the 3D-silicon substrate, maintained on bonder chuck, and InP laser chip compressed by arm).

The bend points of the F=f(z) curves (Figure 100, left) correspond more or less to changes in the bond profile F=f(t) as well as force and displacement speed (dF/dt, dz/dt) in the bonder dynamic (Figure 100, right). Currently, it cannot be excluded that these changes are also related to some drives of the bonder regulation system (counter regulation since near the target force), but, curiously, for the red domain, the flip chip arm displacement basically fits closely with the topography to be overcome on the chip to correctly bond the laser chip, i.e. to bring the chip into contact to the z-stop.

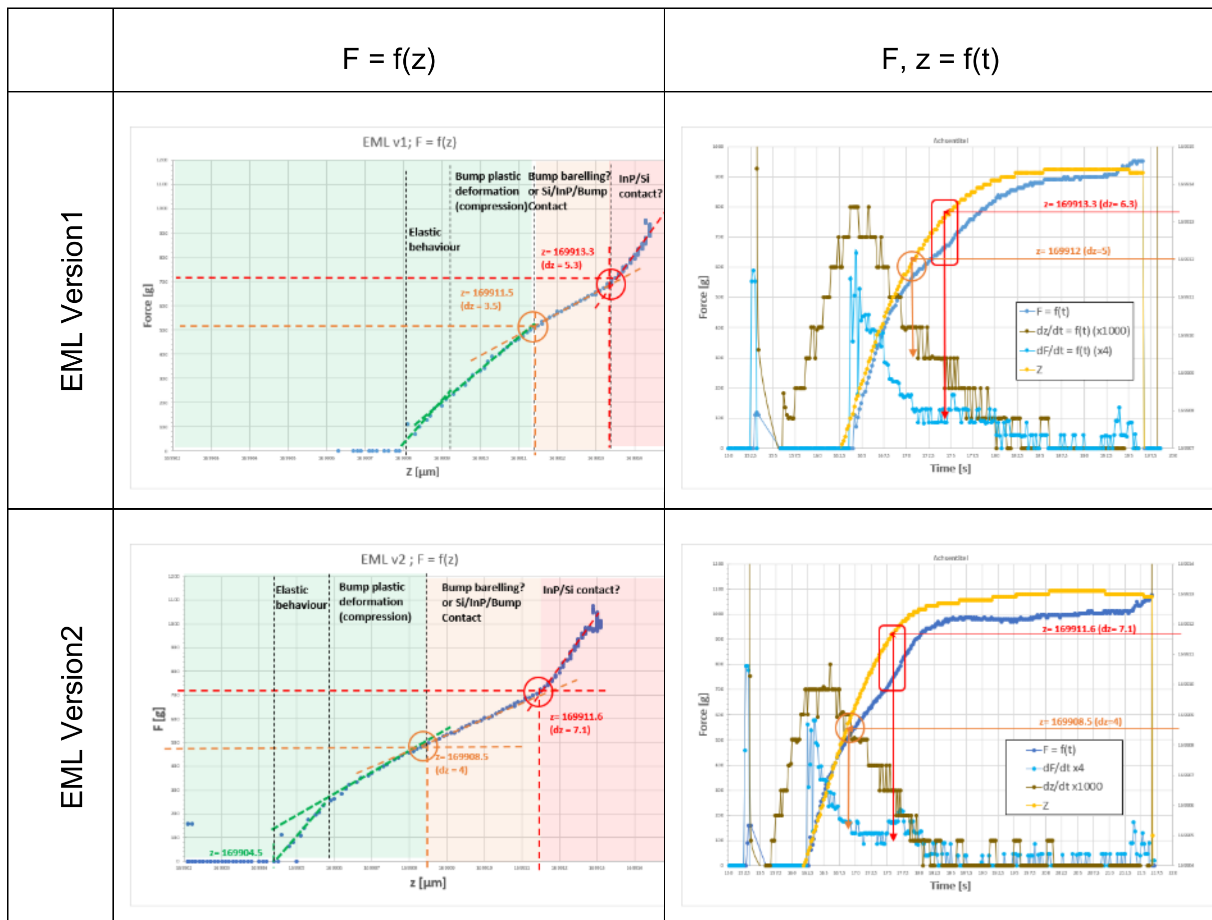


Figure 100: Analysis of Flip chip Process monitoring files: left: force vs. bonder arm displacement; right: displacement (yellow) and force (blue) vs. time

These experiments and results suggest, that an over-regime of compression force further deforms elastically the assembled parts already in hard mechanical contact. When the bonding force gets released, the chip might detach from the thermo-compressed bumps in a reverse elastic effect, leading to disconnection of the thermocompressed gold electrical contacts.

This further implies that an uncontrolled or too coarse-defined bond profile, i.e. including a pronounced over-regime part, will probably result in unconnected devices. This also means, despite the use of vertical stoppers, there is an upper limit in the process window, which is tighter than originally expected.

Self-Alignment Flip chip was exclusively performed in WP4 (Figure 101), new substrates with higher AuSn bumps were fabricated but could not be tested in time. Self-alignment FC trials will be performed out of the project timeframe.

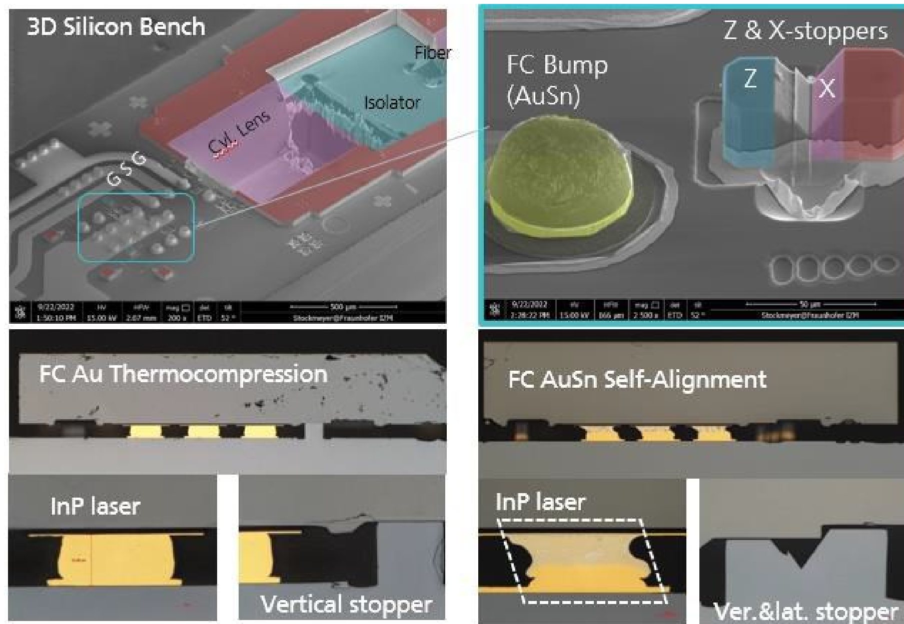


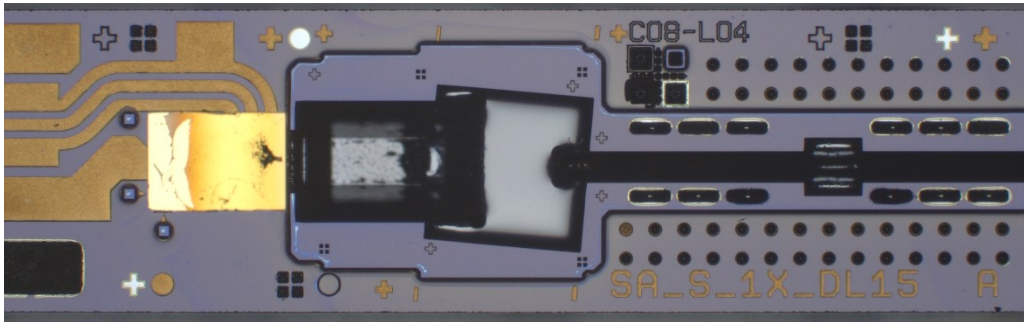
Figure 101 : Flip chip passive alignment (thermocompression and solder self-alignment) tested on 1st generation

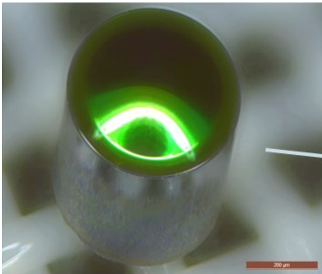
C. Free Space Optic Assembly

The mount of free space optics was also tried at FhG-IZM, despite this task was originally not planed (activity of BESI-AT) to generate fully assembled TX modules by our own (Figure 102). Also Submounts with mounted laser were distributed to BESI-Austria for optic mount with their newly high accuracy bonder "Van Gogh" developed within the APPLAUSE project. However, none of the entirely assembled TX submounts (sample of FhG-IZM shown in Figure 103) were coupling with the Single Mode Fiber (SMF), neither from Fraunhofer IZM nor from BESI-AT.

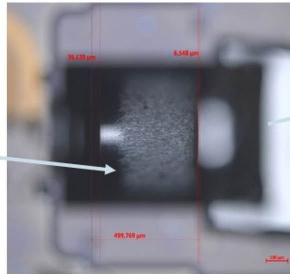
It is hardly believed, the root cause resides in decentering of the Lens: its groove was dimensioned for 500+5µm tolerance (fabricated V-groove width of 623 µm +/-0.5 µm for 624 µm targeted for lens diameter 505 µm with optical axis lying at -4 µm, i.e. stopper level), the parts purchased and provided by Dustphotonics (DPH) were 496+/-1 µm implying an inevitable vertical offset of the lens of ca. -7 to -8 µm from the bench optical axis, when lens sits mechanically in the groove by gluing. Correction trials by pulling the lens up during assembly, to compensate the offset, were all unsuccessful: even @+/-1µm precise lateral placement of the lens and @ -5 µm in vertical direction (best result achieved at FhG-IZM), no light could be coupled into the SMF. The adhesive of the lens by surface tension pulls always the Lens back into the groove even by maintaining the lens at height during adhesive cure. A special lens tooling for holding the lens during bonding would have been necessitated. It must be mentioned that non-destructive metrology of optics assembled by BESI-AT revealed even a lateral and vertical misplacements of up to 10 µm. In their case, the lens was sitting to high (BESI-AT had special tooling developed in the project for lens handling).

The EU Report/Deliverable D5.3- Report on single-mode sub-module - gives further insight on the work performed.

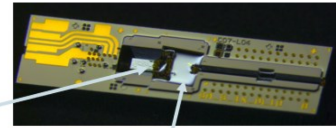


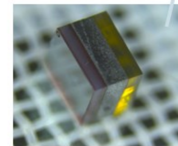


Cylindrical Si-Lens (D=500 µm)



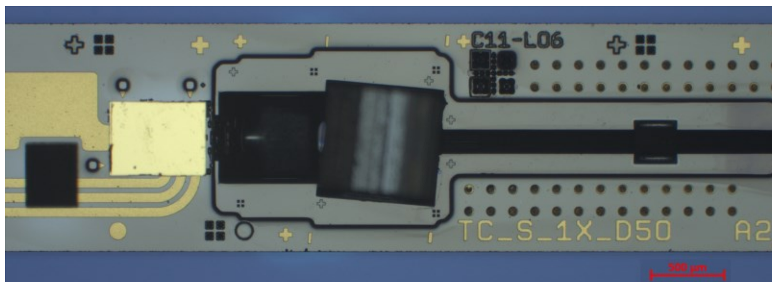
Lens in groove, passive aligned ~1µm
First Test

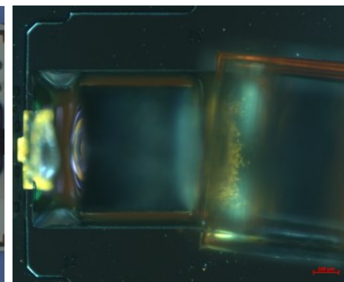


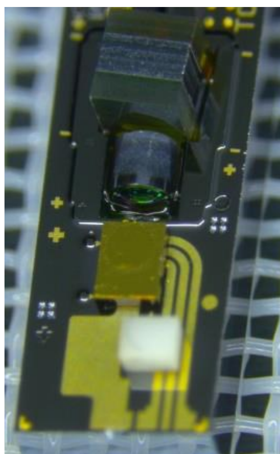


Garnet Isolator

Figure 102: EML device flip chip mounted on 3D silicon optical bench and free optic elements to assemble a Transceiver submodule







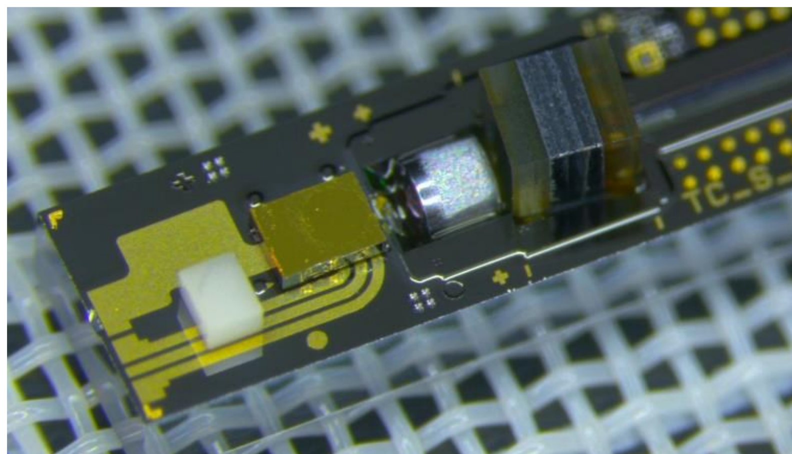


Figure 103: first TX sub-element fully passively assembled at Fraunhofer IZM, inclusive lens and isolator on 2nd substrate generation

Task 5.4 UC4 Packaging processes (cardiac monitoring system)

Task: 5.4.1 Flex on Patch Integration for functional assemblies

Task 5.4.1 a) and b)
a. Flexible Module with integrated Sensor and ICs
b) Stretchable functional module

FhG IZM has layouted the flex for the functional demonstrator, which carries multiple components forming a SiP: the MUSEIC, the Flash Memory IC, a double LED, an infrared diode, an accelerometer, a voltage regulator, ESD protection devices as well as several passive components. Since the MUSEIC is not available as wafer and only one wafer with Flash memories is available, it is not possible or has high risk to fail, if the approach of extreme thinning and chip embedding would be used.

Based on this, the technology approach for the functional flex module changed to a solution were the chips are not extremely thinned and embedded into the flex. Instead of this, the ICs have been assembled by flip chip with studbumps, together with the other components onto the surface of the functional flex. The flex hosted the same components as the molded SiP version from Boschmann in the EU-Consortium. Figure 104 shows the schematic cross view of the intended build-up of the flex. It includes two internal routing layers as well as a top and bottom pad layer. The bottom side pads will be used to contact the flex SiP later with the stretchable patch in the next integration level (TPU embedding).

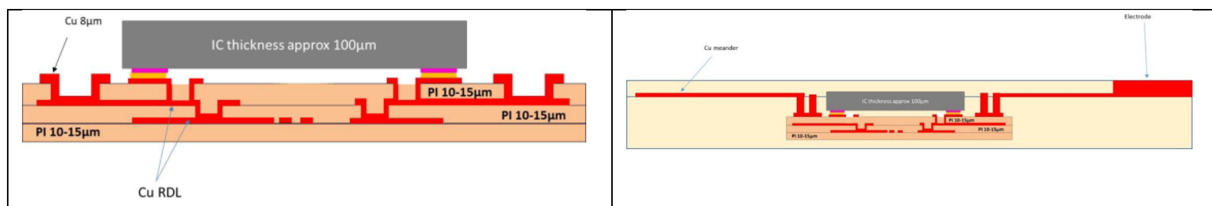


Figure 104: SiP integration change to active device surface mount on HD-thin flex (left) followed by TPU embedding (right).

A. Thinfilm Flex

The fabrication flow for thin film flex is adapted from wafer level redistribution technology and is schematically shown in Figure 105. The process starts at glass wafers of type Borofloat33 with a thickness of 500µm to 700µm on which a polymeric release layer is coated. On top of the release layer of 3-5µm thickness a first polyimide layer of 10 µm thickness is coated and cured without any structuring. The condition corresponds to pictures 1a and b. Now, a first routing layer is fabricated by semi-additive copper technology, which includes sputtering of a seed layer, photo resist lithography, copper electroplating with thickness of 3-5µm, resist removal and seed layer etching (picture 2b of Figure 105). In case that ultra-thin ICs should be embedded into the flex local alignment marks are created by structured etching of the seed layer utilizing another photo lithography step. If the ultra-thin ICs are supplied without die bonding adhesive on their back side, adhesive depots are created directly on the surface of the polyimide by spin coating lithography and dry etching (2a/b)

In the following process sequence, a further polymer layer is realized. The polymer is photo sensitive and structured directly by lithography. Also this routing layer is created by semi-additive copper technology and can have a thickness of 3-5 µm. In case that no ICs are embedded in the flex up to four routing layers were demonstrated. In the standard technology, the routing can have a pitch of 20 µm with a trace width of 10 µm. With the presence of embedded ICs so far only the schematically shown two routing layers were demonstrated. The pads are also created by semi-additive structuring and can be made of Cu, NiAu, Au or CuSn for soldering. In this case Cu/Ni/Au was used.

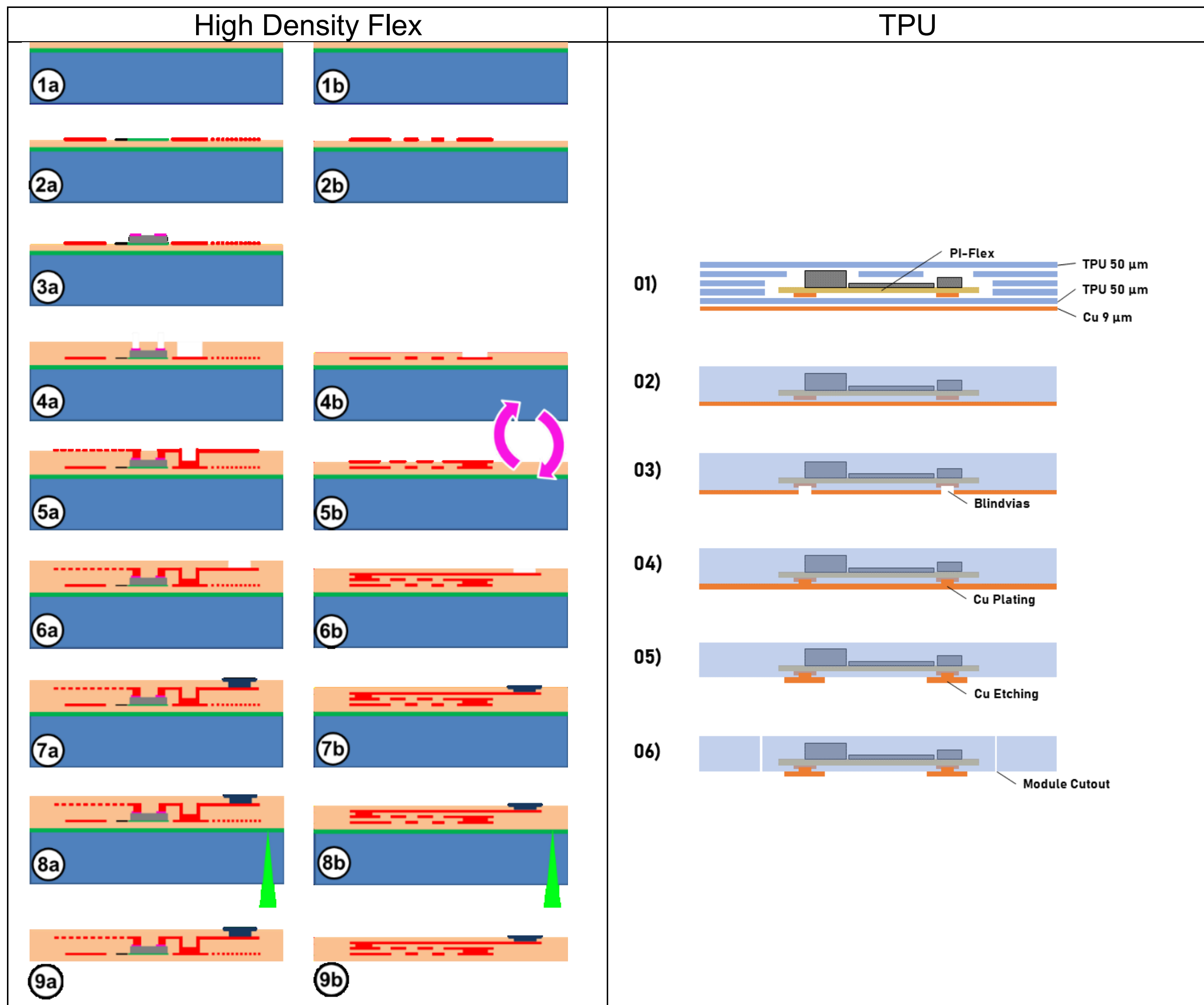


Figure 105: Left: Process flow thinfilm flex - a) with embedded die (WP4) - b) without embedded dies (WP5) – Right: Process flow TPU package

The produced high density flex is shown in Figure 106 (left), after wafer level fabrication and after assembly of components (right). The flex SiP substrate has a total size of 24.6 x 17.6mm2. The total thickness of the flex SiP substrate is 45-50µm.

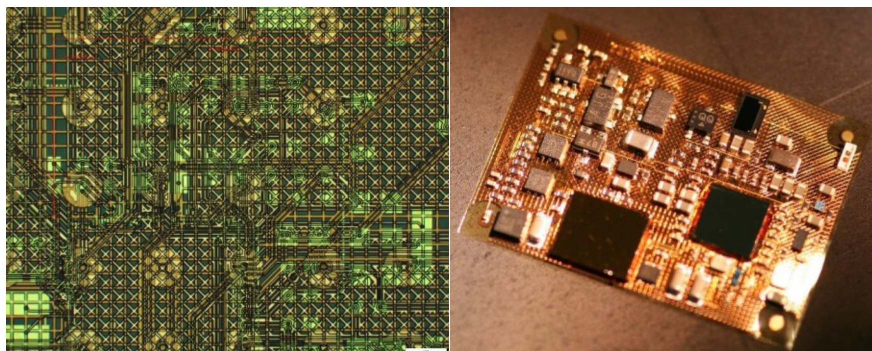
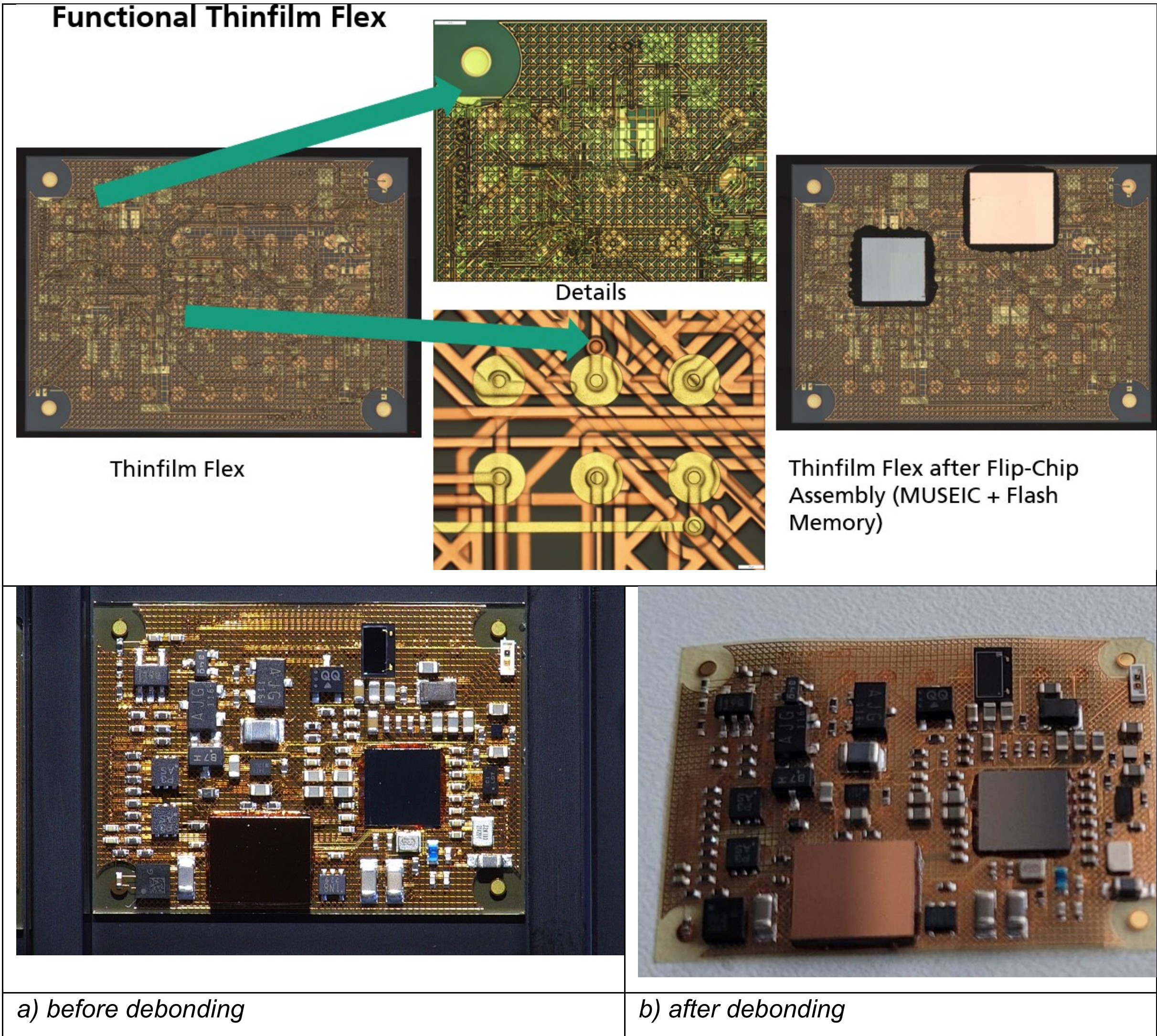


Figure 106: left: High density ultrathin (24,6 mm x 17,6 mm, ca. 40 µm thick) polymer flex with 3 RDL copper layers (left) and after entire assembly of SMD components and release from temperature stable flex-carrier (right). Large IOs for TPU embeddding (ongoing) are on the backside.

B. Flex Assembly

The assembly was carried out while the flex substrates were still fixed on their glass carriers. The SMD components were soldered using standard SAC solder in a conventional reflow process. Afterwards the 2 flip chips were assembled by nonconductive adhesive bonding using an SET 150 flip chip bonder.

The thin flex substrate is fully assembled with functional devices and released from its carrier. The fully assembled flex is shown in figure 2 before (a) and after (b) debonding from the glass. The module has exactly the functionality of the two molded SiPs (demo IMEC-NL) in the alternative packaging approach.



a) before debonding	b) after debonding

Figure 107: Thinfilm flex after assembly of SMD components and flip chips

C. Embedding in TPU

TPU processing for encapsulation was carried out afterwards and resulted in a stretchable patch (Figure 111). As the fully assembled flex has a high topography compared to the technology demonstrator with the embedded dies and without SMD components the embedding process is now different and requires additional layers for height compensation. The process flow is shown above in Figure 105. FhG-IZM integrated the additional system components on the patch base material.

The TPU compensation layers were structured by UV laser and the lamination was performed using a short cycle lamination press from Bürkle that allows short cycle times optimised for thermoplastic materials. The vias were also opened with the laser as already described for the technology demonstrator the the thinfilm flex with embedded dies (WP4).

After cutting out (Figure 108), one of these modules has the same functionality as the two molded SiPs in the alternative assembly approach. The module size is 24,5 X 17,5 X 1,38 mm^3. The modules have to be then integrated on the last patch layer.

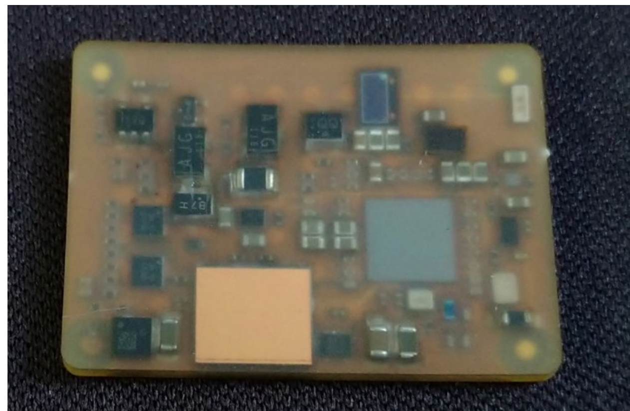


Figure 108: TPU module with MUSEIC and memory flip chips

D. Pach Layer

From the two versions of the patch only the mini patch was realized in the version with the thinfilm module. The patch layer carries the interconnection pads for the TPU modules, the tracks towards the electrodes and the additional components (temperature sensor, antenna and matching network. The assembly is done by SnBi soldering as TPU is temperature sensitive.

The fabrication flow of the patch layer on the panel is shown in Figure 109 on the left) and the final assembly (on the right). The final system is reported in Figure 110.

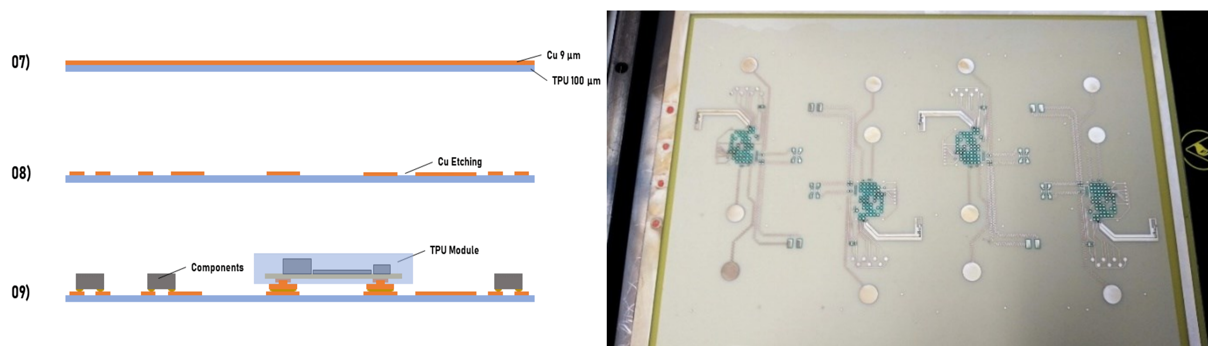


Figure 109: Left: Process flow patch integration. Right: Patch layer on rigid carrier after structuring before assembly

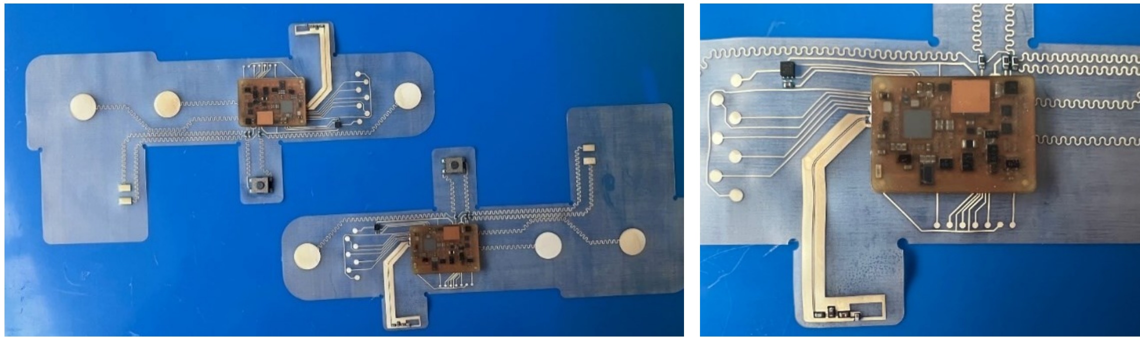


Figure 110: Fully assembled patch with thinfilm module

Electrical function tests were performed and successful, the flex-incorporated Bluetooth antenna was also trimmed for data flow. The samples were then delivered to IMEC for further function tests/verifications.

Together with the integration of the thinfilm flexes in functional patches, FhG-IZM integrated also the molded SiPs of IMEC-NL for the alternative assembly concept of IMEC-NL (Figure 111). For this purpose SnBi solder was used. Jetting parameters for solder application have been determined in short loops. The compatibility of the soldering and underfilling processes with the printed electrodes on the TPU was also verified in shortloops, prior processing final parts.

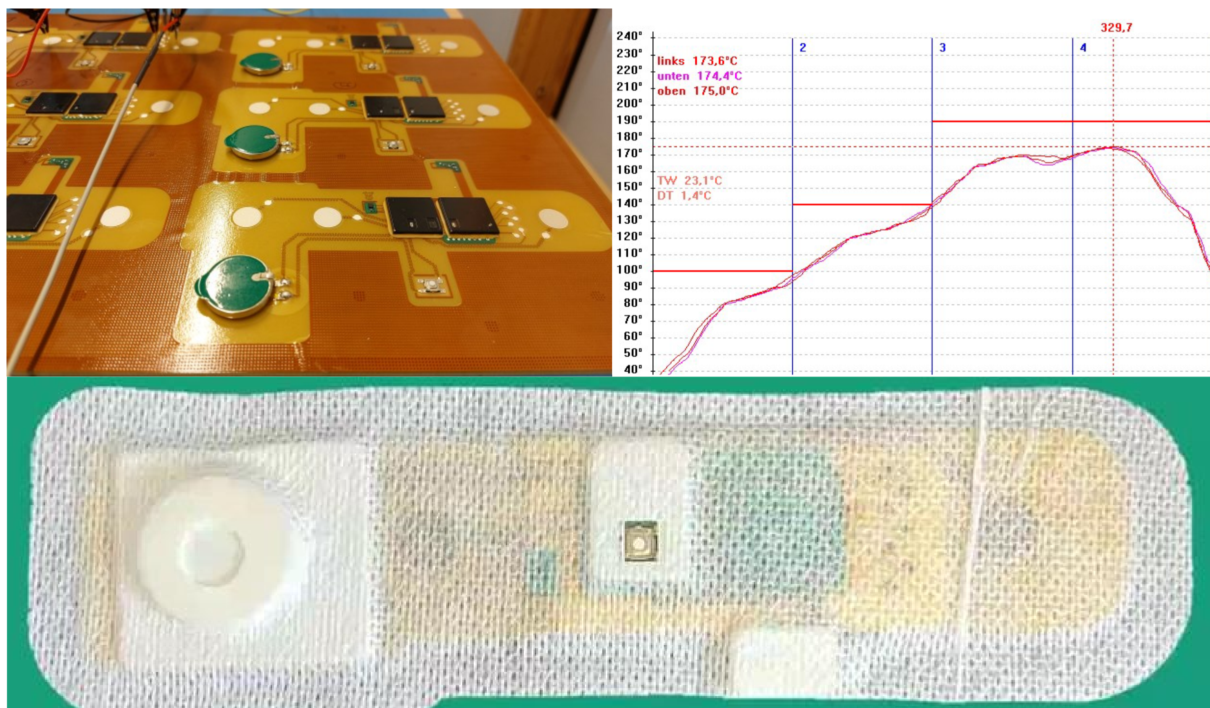


Figure 111: Top: MiniPatch after assembly (still on carrier) and SnBi reflow profile – Bottom: Final patch with molded SiPs

WP6 Testing, Reliability, Failure Analysis & Metrology

Task 6.2 Characterization of electrical and optical properties

a. UC2-related

Within UC2, the Antireflective coating was characterized on Si-Dummy substrate (Monitor CZ Si Double sided polished DSP, ~ 700µm thick) according different single process steps representative of the cap wafer preparation (a.o. temporary bonding, wafer sealing, O2 plasma ashing). The temporary bonding and sealing process affect the ARC due to temperature budget, the provided ARC starting to degrade (crack formation, peeling) by temperature above 300°C. This basic investigation permitted at least to select a temporary bonding with lower thermal load to hinder a pre-damage of the ARC. However the processes tested did not seem to affect its transmission curve in the wavelength range of interest (8-14µm, LWIR), at least on the Silicon of monitor grade as substrate (Figure 112).

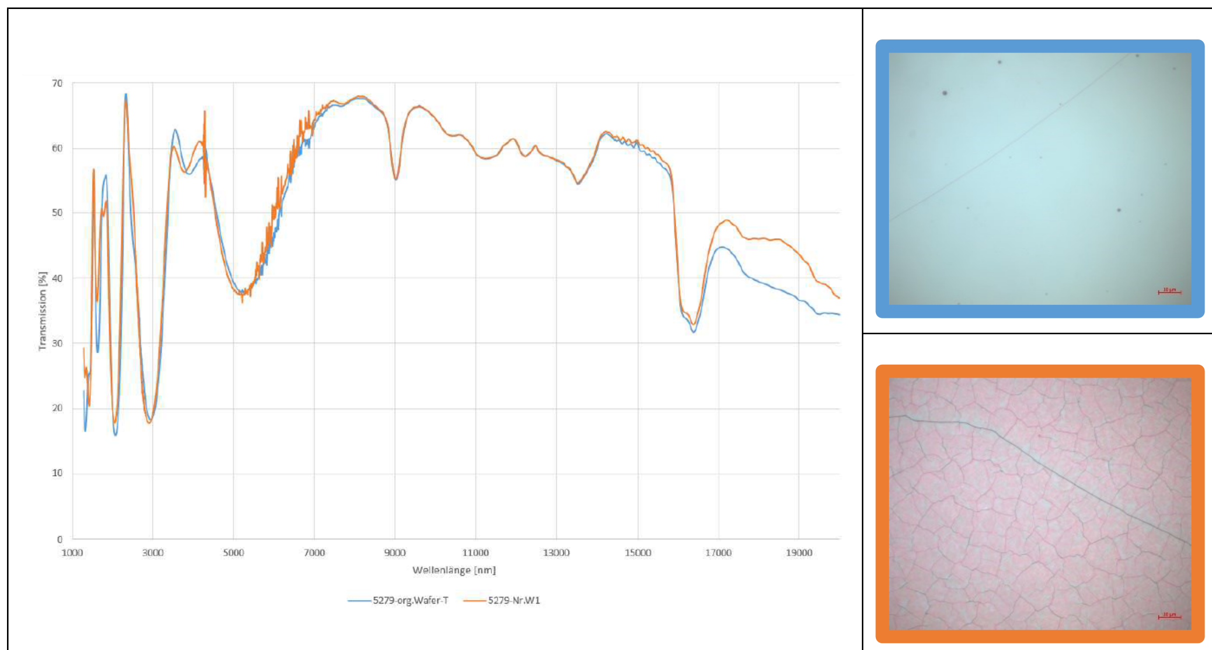


Figure 112: transmission curve (1000 – 20000 µm) of the industrial ARC deposited on 200mm from subcontractor, as deposited (blue) and thermally stressed at 350°C – 10 min (orange) and corresponding surface aspect under light microscope.

In addition, all the pirani resistance of (hermetically) capped die were measured after singulation at Fraunhofer IZM and USN / Norway (Pirani Design, Characterization of reference curve). A vacuum as low as 10^{-1} mbar (~ 100 kOhm on priani #11) could be assessed after full process with getter (see T5.2). Investigation on pirani resistance after wafer encapsulation (ring bonding) and after annealing for 1h under Nitrogen @ 250°C (under temperature of getter activation) and 350°C (Figure 113 and Figure 114) were performed also on singulated die to investigate the potential of further activation of the getter material. A further post-activation seems feasible, a further drop of the Pirani resistance could be measured on hermetical die by comparing the values of “as bonded”.

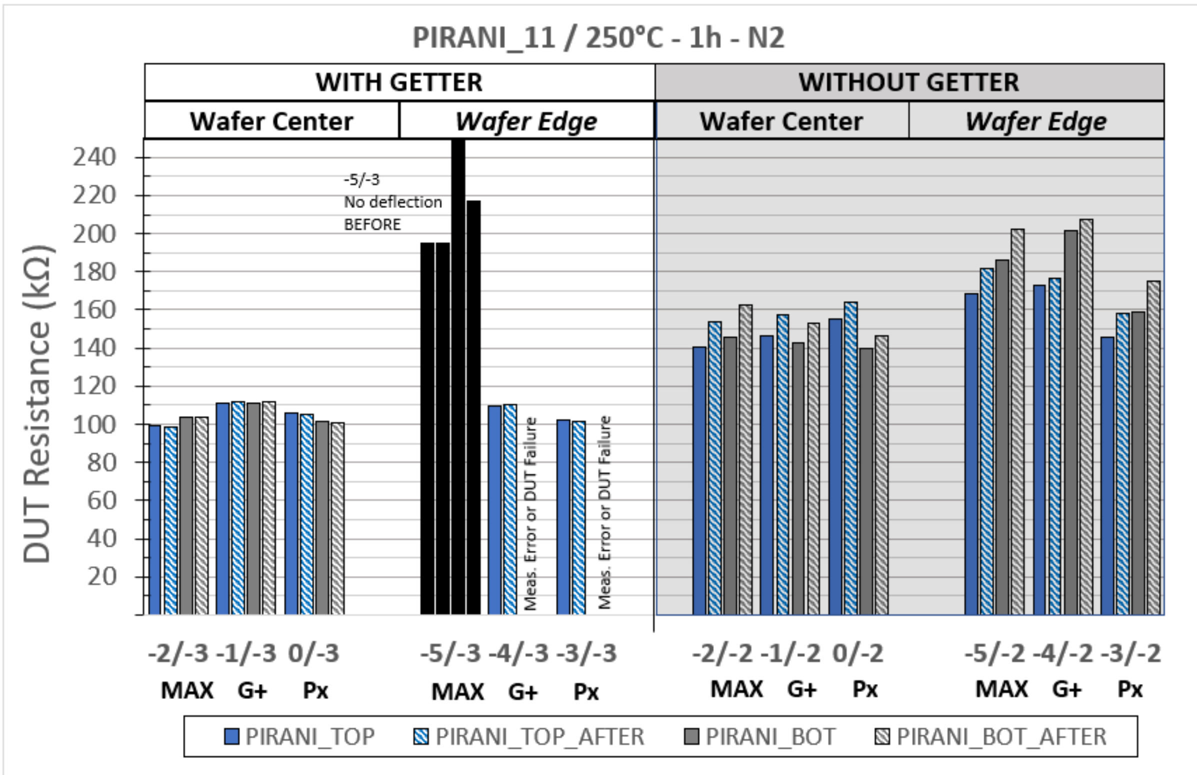


Figure 113: Results of Pirani resistance on singulated die after wafer bonding and annealing at 250°C for 1h.

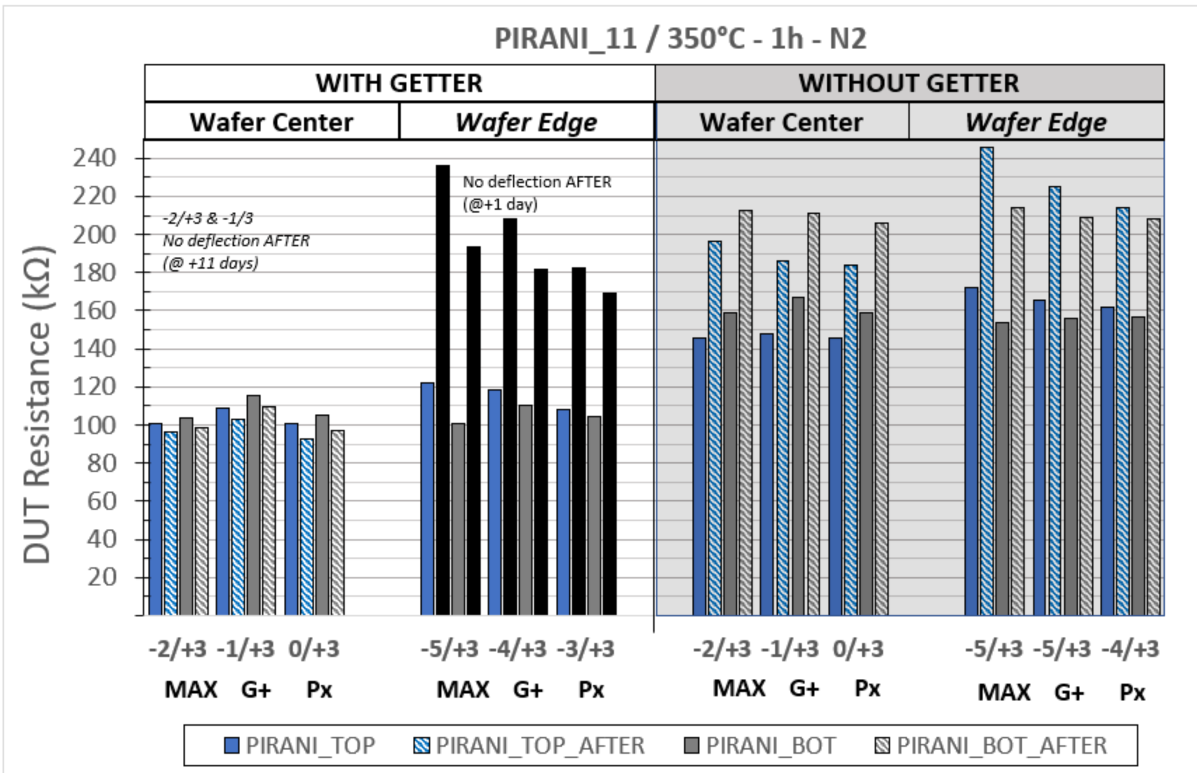


Figure 114: Results of Pirani resistance on singulated die after wafer bonding and annealing at 350°C for 1h.

b. UC3-related

The high frequency behaviour of the gold routing on the low resistivity/standard silicon (<50 Ohm.cm) and high resistivity silicon (>2000 ohm.cm) has been tested (see Figure 115), up to 67 GHz, with S11 and S22 under -20 dbm up to >50 GHz and transmission losses ~ -5 dbm until 67 GHz.

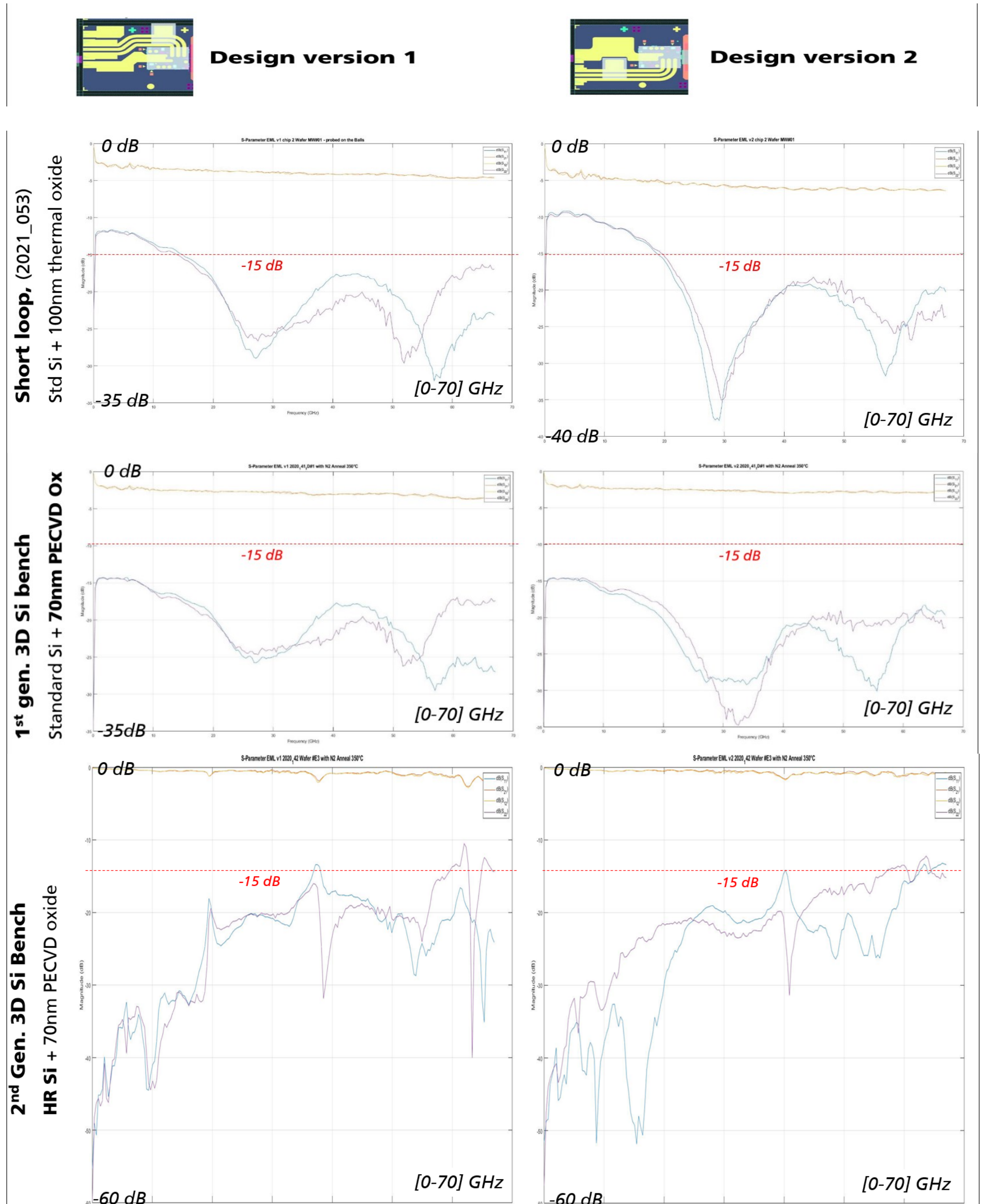
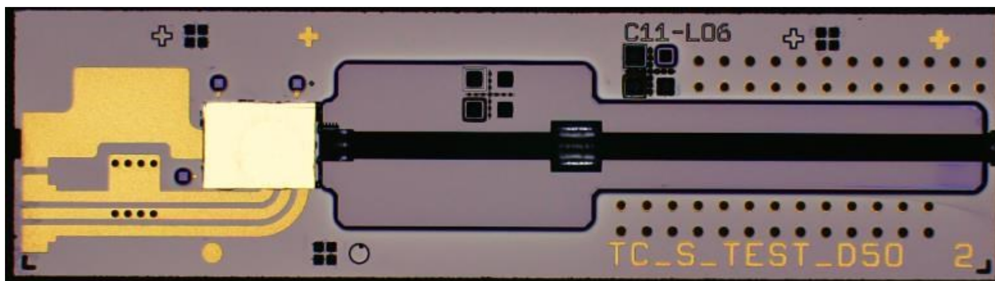


Figure 115: HF measurements of the transmission lines on different UC3 silicon substrates

The results are in accordance with the simulations. Sxy transmission losses are higher on standard Silicon (resistivity < 50 ohm.cm) with an isolation of 100 nm thermal oxide or 70 nm PECVD Oxide (up to -5 dBm), compared to high resistivity Silicon (<-2 dBm) with a PECVD Oxide of ~70 nm (HR Si wafer being on temporary carrier for secured processing, no thermal oxide, thermal budget too high for carrier systems), and reflection losses are all under -15 dBm in HF range above 20 GHz.

Short loop flip chip assemblies were performed to test the laser characteristic curve (IV-Curve), optical power and PAM-4 protocol after flip chip process of laser and decoupling 50-ohm resistor and compared relatively to the “as fabricated” values of laser provider (partner ALMAE, France).

Furthermore, process test assemblies on intermediate/ “simplified” 3D Si bench (Figure 116), ie. with only the flip chip (with mechanical stoppers) and a V-groove for fiber (“Laser-to-fiber” test vehicle, “Fiber-only”) were performed and tested with glass fiber, in order to “physically” assess the flip chip process and the correct postbond position relative to the optical axis of the 3D Silicon Bench. Laser chips were also characterized using this type of test vehicle (Figure 117 and Figure 118).



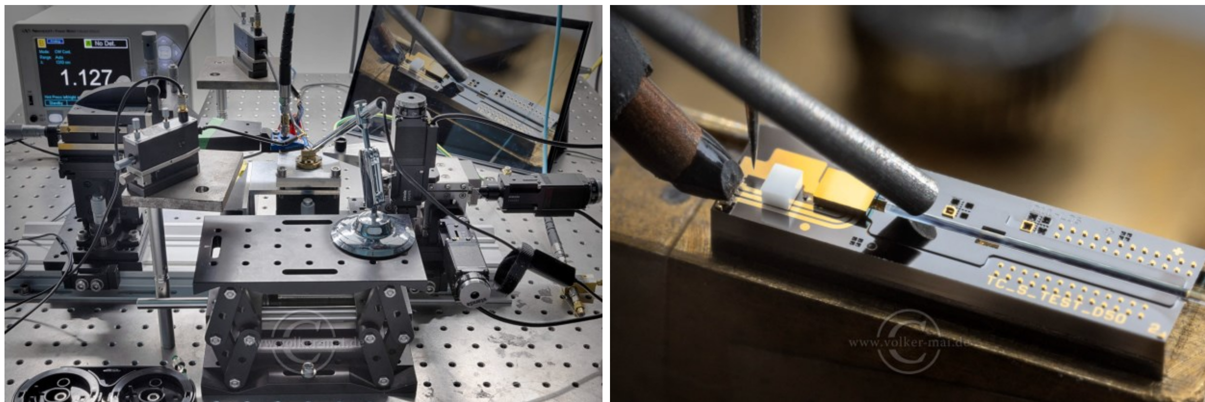


Figure 116: “Fiber-only” test vehicle with precise flip chip thermocompression of EML_v2 (2nd substrate generation)

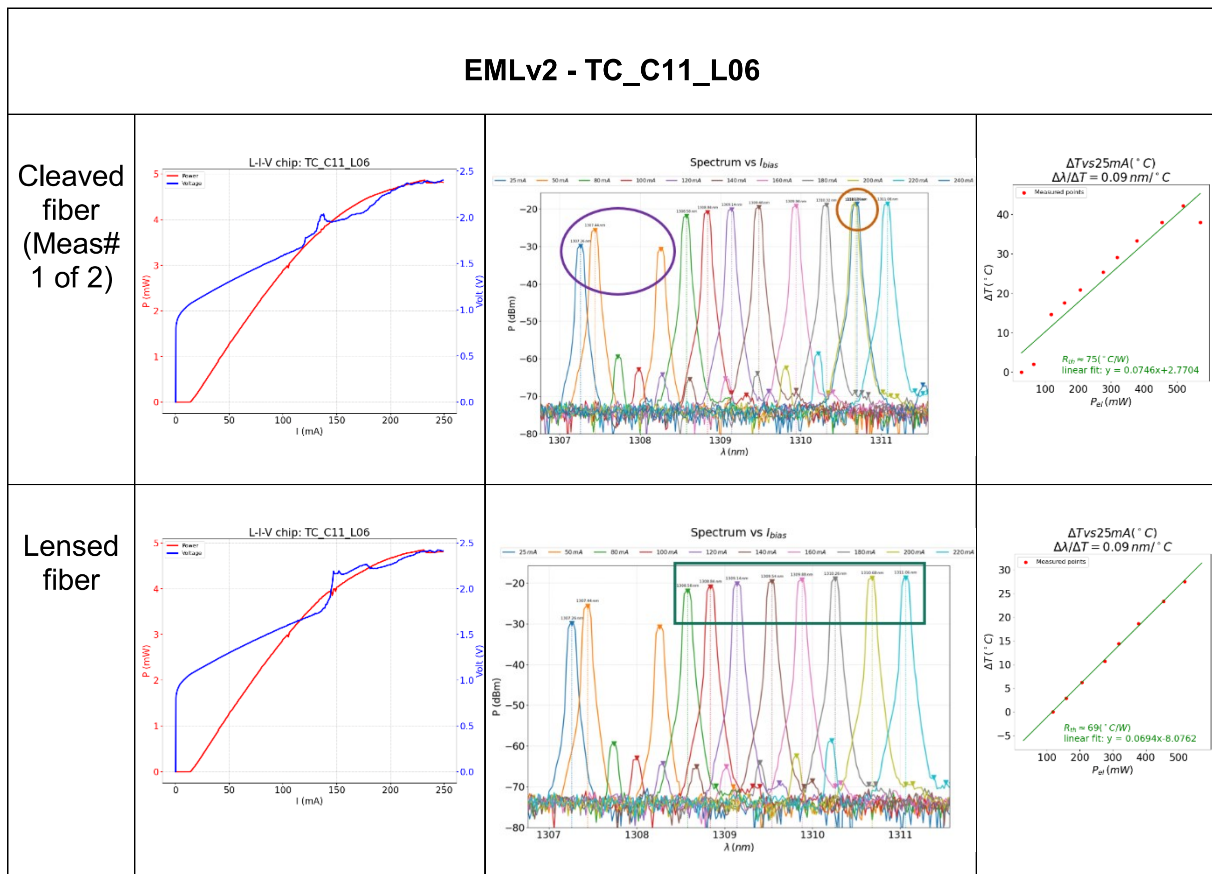


Figure 117: Example of Characterisation results of FC TC EML_v2 with fiber-only test vehicle with 3D silicon of 2nd generation.

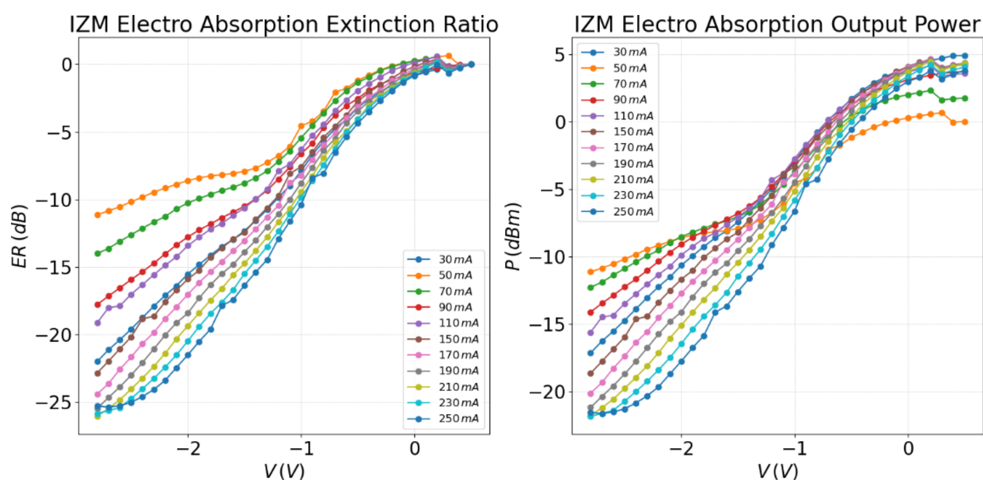


Figure 118: Electro Absorption testing at FhG-IZM

The Flip chip Laser die assembled on vertical stopper by thermocompression present most of the time a VI behaviour with a kink around 150 to 200 mA (Figure 117) A. The reason is unclear, maybe to due crack formation in MQW or stress build into the MQW layer. Another reason could be the heat generated during driving with insufficient cooling, leading to laser failure.

Additionally, first fully assembled parts were also tested with glass fiber, unfortunately without success, either on TX units passively assembled with high precision bonders at Fraunhofer IZM as well as at BESI-AT.

c. UC4-Related

The test vehicles with embedded dummy silicon chips for technology development were characterized electrically (see T4.4). Since the results were positive, the samples were further used for reliability tests (see T4.4 & T6.3)

Task 6.3 Qualification and reliability

a. UC2 related

The pirani MEMS were tested after hermetical capping and dicing and also after thermal annealing of the silicon-based packages (see 6.1).

b. UC3 related

Unfortunately, due to cumulative issues and delays in substrate fabrication and assembly, the prepared samples did not reach the necessary maturity to perform Q&R tests in a relevant manner.

The bonding strength of EML after flip chip was tested by shear testing on the 3D Si Bench after thermocompression on dedicated test-substrates (ie. no mechanical stoppers).The shear behaviour was investigated, to find a compromise between the bump deformation and a sufficient bond resistance to shearing. The InP chip tends most of the time to break during shear testing due to its fragility and susceptibility to fracture (+ InP die sidewalls irregularities formed during singulation by cleaving, sites prompt to crack formation). The shear force varies from with the shear direction, but maximal shear forces from 50 MPa to ca. 200 MPa were measured using bumps of 50 µm diameter, indicating a satisfying bond behaviour (Figure 119).

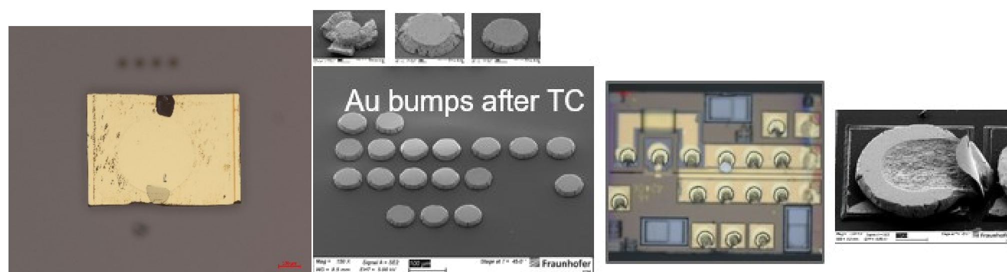
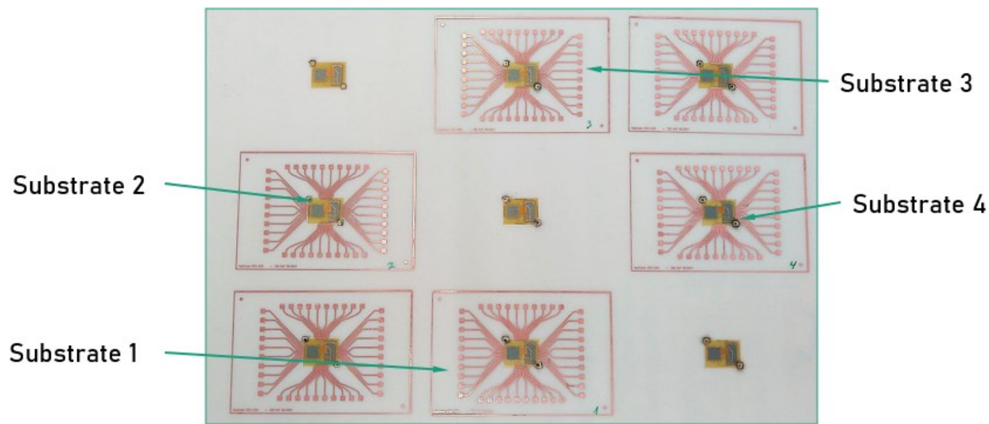


Figure 119: TC tests of Au bumps for bump design (a.o. bump deformation/buckling, shear testing).

c. UC4 related

For the UC4 Dummy test vehicle, complete Routing integrity of dummy embedded chips in flex and then flex embedded in patch has been verified using test structures (daisy chain like, DC) as well as the single via (Kelvin test structures, K), Figure 120. Similar results were obtained after humidity tests (85°C/85% rel. hum) and thermal cycling (0..80°C), after 500h and 1000 thermal cycles, indicating no dramatic deviations or weak points in the patch as well as in the flex routing (part comprising the embedded thin chips).



	DC1	DC2	DC3	DC4	DC5	DC6	DC7	DC8	DC9	DC10	DC11	DC12	K1	K2	K3	K4	AM	AFab
Substrate 1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Substrate 2	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Substrate 3	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Substrate 4	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Figure 120: verification on 4 substrates of electrical routing integrity with dummy test structures (DC: daisy chain, K: 4-point) after thermo-cycling 0-80°C / n=1000.

Task 6.4 Failure analysis

a. UC2-related

In the frame of UC2, physical analysis (T6.4) were undertaken not only for bond results evaluation but also all the sample fabrication. For example, to find a process for applying a sacrificial layer and for releasing it after wafer processing, just prior hermetic sealing, as shown in T5.2. Cross-section, FIB, SEM permitted also to inspect the quality of the sidewalls in the fabrication of the silicon frame (T4.3, T5.2) and bonding of germanium lid on silicon (chip level feasibility evaluation).

As reported above, the wafer sealed parts were inspected in multiple non-destructive manners (optical and infrared microscopy, profilometry/cap bending, X-RAY, SEM/EDX, C-SAM) as well as destructively (metallographic cross-sections) to inspect the bonded sealing rings. Water permeation tests for gross-leak checks were also performed. The encapsulated Pirani MEMS were also characterized using wafer prober, to extract the vacuum level inside the wafer sealed samples. Herewith, a packaged vacuum of 10^{-1} mbar can be stated.

b. UC3-related

For the 3D benchs, extensive investigations were performed all along the process developments to support the developments. Optical microscopy, SEM, FIB cuts, Cross-sections, 3D-Topography measurements (a.o. Stoppers, Bumps, surface of InP lasers) were used.

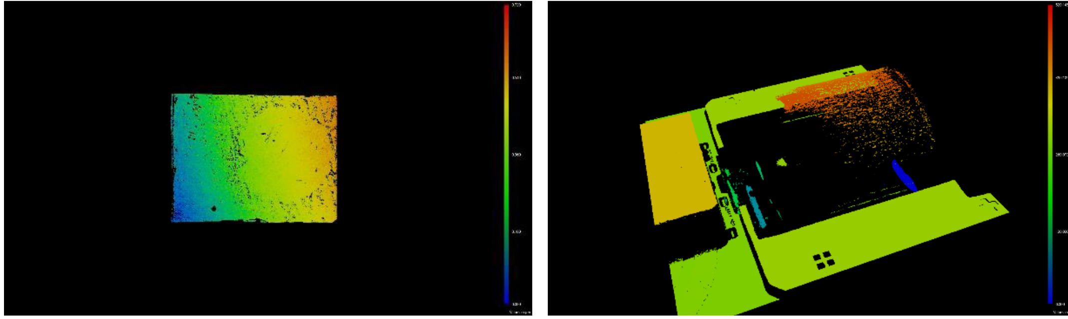


Figure 121: Examples of precise 3D metrology – Left: backside planarity to flipped thermocompressed laser on 3D Silicon bench (<0.7 µm) () – Right: lens glued in groove supporting the assembly of 2nd substrate generation

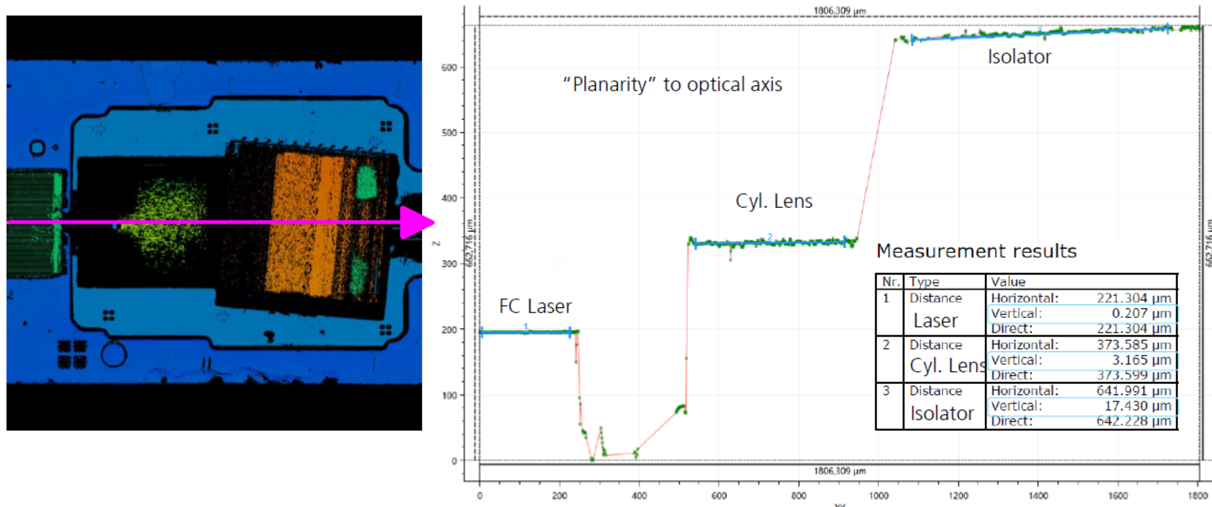


Figure 122: example of precise 3D-Metrology – Planarity & relative heights over a Fully assembled TX unit (lens and isolator assembled by BESI-AT)

c. UC4-related

In a similar way, the developments in UC4 were supported with destructive and non-destructive inverstigations to assess the single process steps. One of the critical points for interconnect is the via opening and metal plating within to form a metal routing. Figure 123 give some impressions of this aspect, with cross-section onto via contacts of an embedded die as well as within the flex routing layers.

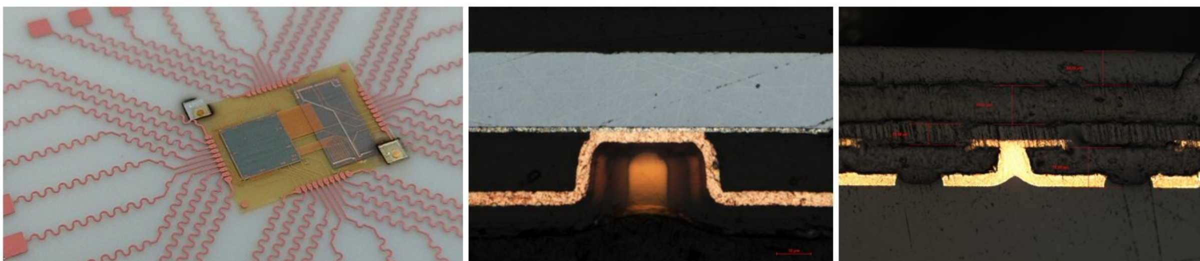


Figure 123: via inspection with cross-sectioning within thin flex

WP7 Fabrication and Validation of Use Case Demonstrators

Wafer level packaging processes were developed:

1. to deposit AuSn bond rings on MEMS device wafers without damaging MEMS microbolometer,
2. to fabricate Monolithic silicon cap Wafers, with low TTV and robust to undergo advanced packaging, including die attach, wirebonding, molding and soldering
3. to fabricate hermetic hybrid silicon caps incorporating extended/maximized cavity depth (~700µm) based on flat silicon lid wafers (with backside antireflective coating) bonded to etched-trough Silicon frame wafers with AuSn seal rings,
4. to seal at wafer level large device MEMS (>12mm chip size) with silicon cap wafers

with the target of an industry-oriented processing for wafer level vacuum hermetic sealing of MEMS device wafers (Figure 124).

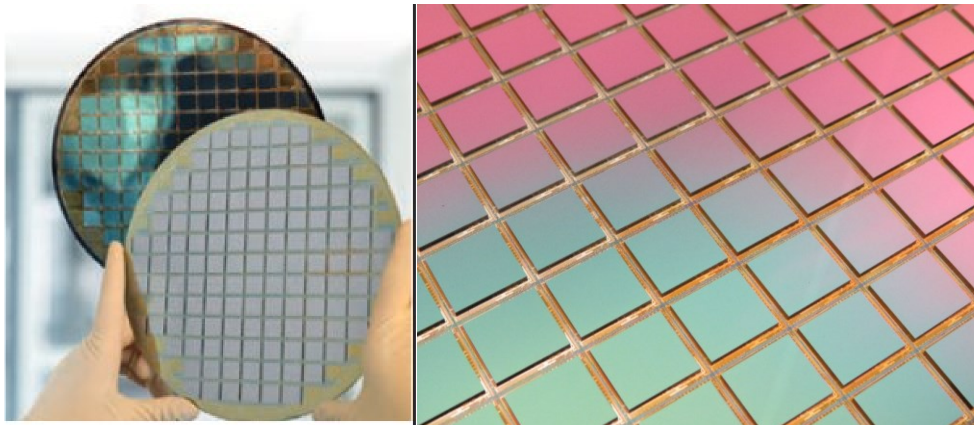


Figure 124: 200mm Bolometer Device Wafer hermetically sealed (AuSn wafer bonding) with caps integrating LWIR anti-reflective coating (ARC) and getters, after cap singulation

Task 7.3 UC3 demo, fabrication and validation

A. Wafer Level Fabrication (200 mm) of 3D silicon submonts/benches for photonic applications

Due to withdrawal of Dustphotonics, partner integrating the Transmitter /TX (IZM) and the Receiver / RX (ALBIS, Switzerland) for the use case, demo work was only performed on submodule basis, with support of NVIDIA (new demo partner, in replacement of DustPhotonics).

In APPLAUSE-UC3, in regards of fabrication of high-speed transceiver (TX) by full passive optical alignment for coupling into SM-fibre Fraunhofer IZM developed and fabricated a 3D Silicon optical bench (Figure 125), with the specific focus on integration of discrete optical devices by full passive optical alignment.

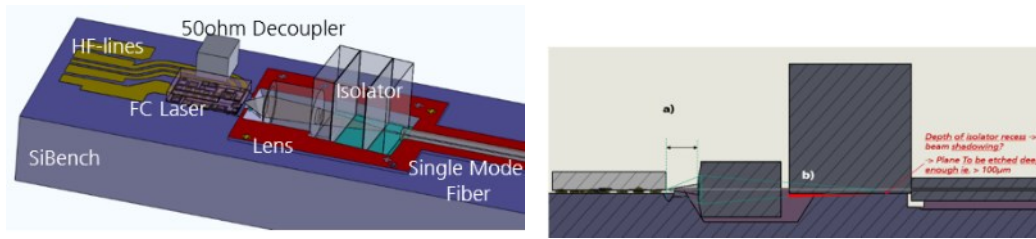


Figure 125: 3D Silicon optical bench for transceiver (TX) submodule

For this purpose, special features were micromachined on silicon by wafer level processing on 200mm wafer scale, creating 3D mechanical stoppers, grooves and recesses (Figure 126) for the passive assembly along the entire optical axis.

The Silicon bench incorporated also thick metallisation layers, with a gold galvanic layer for HF-Routing (GSG lines) and Au or AuSn micro-bumps for precise passive flip chip mounting of InP EML / laser dies.

The 3D Silicon bench should permit the optical integration of flip chip lasers, lenses, isolators and Single mode fibers in an entire passive scheme, using high accurate bonder and/or specific mechanical arrangements.

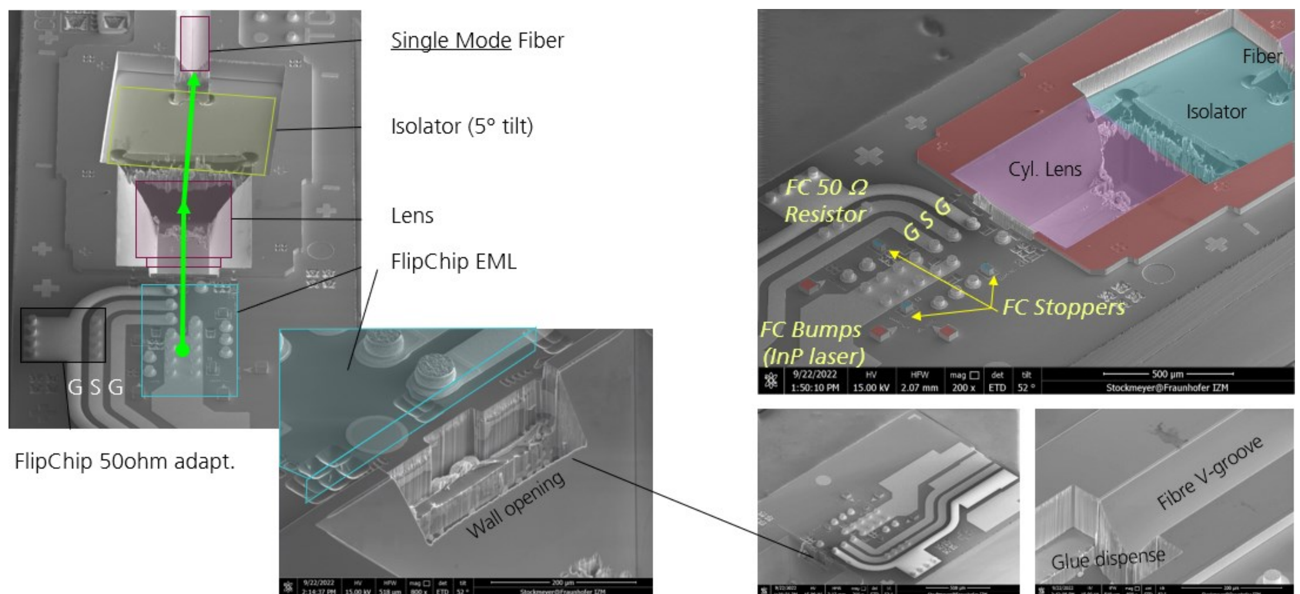


Figure 126: 3D silicon optical bench for passive alignment (FhG-IZM)

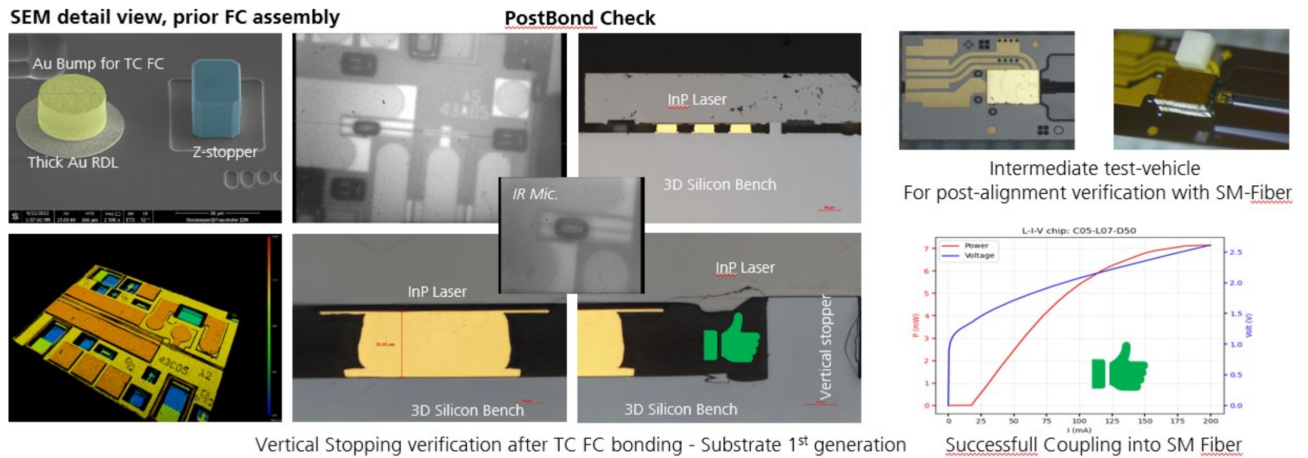
B. Passive Alignment of FC InP laser (EML) by precision flip chip bonding

Besides the substrate manufacturing and all the corresponding wafer level process developments, two flip chip technologies were implemented on the silicon bench for precise passive alignment of the laser devices:

1. FC Thermocompression (Figure 127) with plated gold microbumps, with passive alignment using
   a. lateral alignment, machine assisted recognitions

b. vertical mechanical stoppers for the correct matching with the optical beam axis, with compression of the Au bumps

2. FC Self-alignment (Figure 128) with plated AuSn solder bumps, with passive alignment using
   a. 3D micromachined mechanical stoppers,
   b. Self-alignment by reflow of AuSn solder bumps, bringing the component on the 3D stoppers



→ Validation of concept with 1st generation of 3D Si-substrates

Figure 127: passive aligned flip chip laser with thermocompression (FhG-IZM)

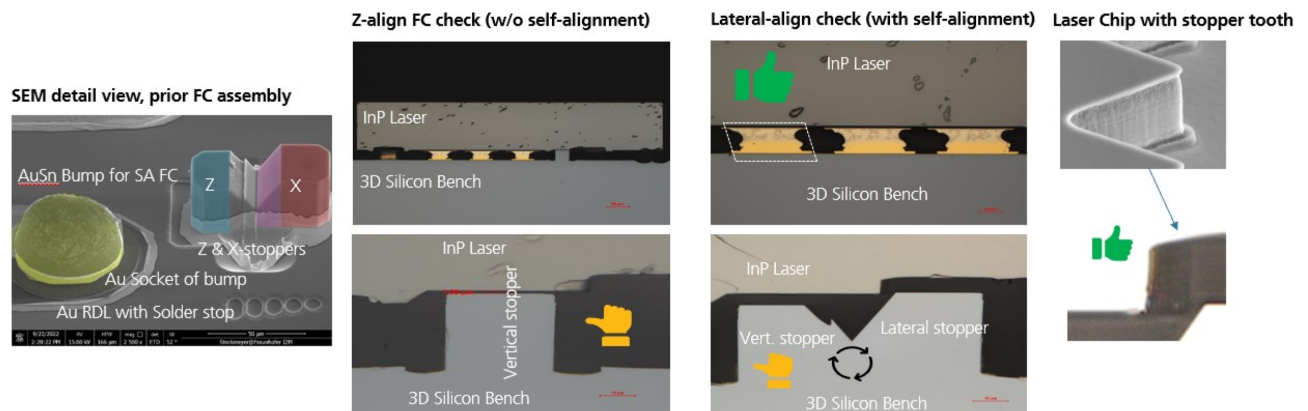


Figure 128: passive aligned flip chip laser with solder self-alignment (FhG-IZM)

The flip chip technologies should enable the precise bonding of the EML device on 3D the silicon bench (in process evaluation) for assembly of single-mode emitting sub-module. The assembly of the free optic elements (lens, isolator) should be then implemented by BESI with their APPLAUSE highly precise bonder when all the correct optical components are available. Tests using mechanical features will be also addresses in parallel (see picture below of pre-trial of lens on 3DSiBench)

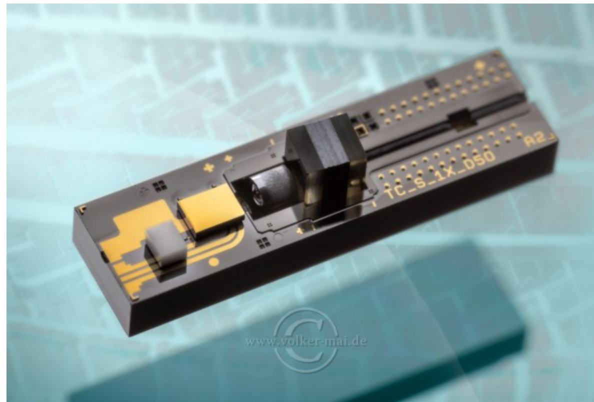


Figure 129: example of fully passive assembled Transmitter Unit composed of a flip chipped InP laser, its 50 ohm decoupling resistor, a cylinder Lens and an optical isolator.

Task 7.4 UC4 demo, fabrication and validation

In UC4, the Flex embedded Patch of IZM (Figure 130) has been successfully fabricated by end 2022. Results on characterization by partners are pending at report writing.

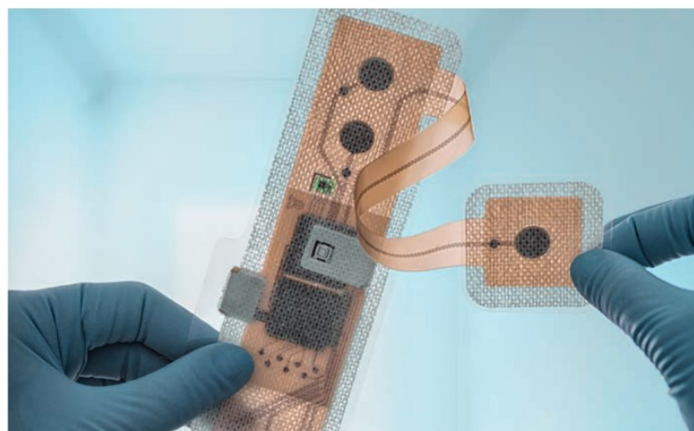


Figure 130: Multisensor patch (ECG, PPG, impedance, pneumography, movement) on TPU

General Conclusion

In the frame of the project, all tasks were fully executed without major deviations as described in the report. The packaging technologies dedicated to each of the Use Cases could be successfully developed and leaded to acceptable to noteworthy results:

1. Within UC2 (Wafer level packaging for low cost IR camera), the wafer level hermetical sealing of MEMS-based microbolometer could be demonstrated with AuSn bonding up to a seal yield evaluated to over 95 % on 200 mm MEMS device wafer for large chips (>10x10 mm²), with a packaged vacuum in the range of at least 0.1 mbar (end of the sensitivity range of the Applause-specific Pirani sensor).
2. For the photonic application UC3 (full passive assembly of transmitter unit), where very high precision is the primary key aspect, the fabrication of the 3D substrates (Mold & Silicon) could be performed on 200 mm wafer scale with decisive learning curves, whereby the silicon-based version would need undeniably further ameliorations based on the lessons learned from the project. Flip Chip on 3D Stoppers was experimented in thermocompression with high precision FC Bonder and in self-alignment with AuSn solder, the first showing promising results, the second remaining in experimenting level. The precise full passive assembly of entire opto-transmitter units (TX) remains nevertheless over challenging, since none of fully passive assembled parts could be effectively tested, despite all efforts spent on processes and inspections.
3. The UC4-related developments (cardiac monitoring system with polymer embedding), on high density flex, thin chip flex embedding and TPU embedding, lead to a first technologic-convincing passive test vehicle as well as a functional system for the application field, the latest to be tested by project partners.

Related EU Deliverables

The deliverables, where IZM was involved as leader or participated, are listed below.

Deliverable no	Deliverable name	Lead Participant Short Name	Type	Dissemination level	Due (EU)	Status
2020						
D1.3	Risk management plan	ICOS	R	CO	M06	Submitted
D1.6	Intermediate periodic project progress report - M6	ICOS	R	CO	M06	Submitted
D2.2	Requirements and specifications for UC2: Low cost thermal imaging system	IDEAS	R	CO	M10	Submitted
D2.3	Requirements and specifications for UC3: Passive fibre alignment for single mode transceivers	DPH	R	CO	M10	Submitted
D2.4	Requirements and specifications for UC4: Cardiac Monitoring Patch	Precordior	R	CO	M12	Submitted
2021						
D1.7	Intermediate periodic project progress report - M18	ICOS	R	CO	M18	Submitted
D3.5	Design of a pick & place machine and optical package support structures	BESI AT	R	CO	M21	Submitted
D3.6	Optical package design for a 400Gb/s transceiver	DPH	R	CO	M24	Submitted
D4.7	Geometrical precision of molded 3D substrates	FhG-IZM	R	CO	M21	Submitted M24
D4.6	Report on flexible/stretchable integration technologies	IZM	R	CO	M24	Submitted M27
2022						
D1.8	Intermediate periodic project progress report - M33	ICOS	R	CO	M33	Submitted

D4.2	High-precision photonic packaging	BESI-AT	R	CO	M30	Submitted M40
D4.3	Bonding Processes	EVG	R	CO	M28	Submitted M40
D5.2	Report on packaged microbolometer	IZM	R	CO	M40	Submitted M42
D5.3	Report on single-mode sub-module	IZM	R	CO	M40	Submitted M42
D5.4	Report on packaging of a cardiac monitoring system	IZM	R	CO	M40	Submitted M44

+ Additional/volunteer Participation to D7.2 and D7.3 (Reports on UC2 and UC3 demonstrators)

For orientation:

- *EU-Level M01 = Mai 2019*
- *EU-Level M12 = April 2020*
- *EU-Level M24 = April 2021*
- *EU-Level M36 = April 2022*
- *EU-Level M42= Oct. 2023*

Auflistung der auf deutscher Sprache wiedergegebenen Arbeitspakete und Aufgaben/Tasks aus dem Projektantrag

AP1 Management

Task 1.1 Technische Koordination

AP2 Anforderungen und Spezifikationen

Task 2.2 Anforderungen und Spezifikationen für Applikation 2 (Kostengünstige Wärmebildgeräte)

Task 2.3 Anforderungen und Spezifikationen für Applikation 3 (Passive Faserausrichtung für Single-Mode-Transceiver)

Task 2.4 Anforderungen und Spezifikationen für Applikation 4 (Herzüberwachungssystem)

AP3 Design, Modellierung & Simulation

Task 3.2 Entwurf für Applikation 2 (Kostengünstige Wärmebildgeräte)

Task 3.3 Entwurf für Applikation 3 (Passive Faserausrichtung für Single-Mode-Transceiver)

Task 3.4 Entwurf für Applikation 4 (Herzüberwachungssystem)

AP4 Equipment, Prozesse und Softwarekomponenten

Task 4.2 Hochpräzise Aufbau- und Verbindungstechnik (AVT) für Photonik

4.2 a) Testvehikel für die hochpräzise Bondtechnik

4.2 b) Entwicklung einer Flip-Chip Präzisionsmontage

Task 4.3 Verbindungstechnologien für empfindliche optische Komponenten

4.3.1 Hermetische Verkapselung auf Wafer-Level

4.3.1 a) Sensor-Wafer Präparation

4.3.1 b) Siliziumrahmen

4.3.1 c) Rekonfigurieren von Germaniumfenstern

4.3.1 d) Bonden Dreierstapel

Task 4.4 Medizinische und biokompatible AVT für die Photonik

Task 4.4.1 Technologieentwicklungen für flexible/dehnbare Substrate mit ultra-dünnen Komponenten

Task 4.4.1 a) Integration von dünnen Chips in flexible Polymerlagen

Task 4.4.1 b) Planarisierung und Einbetten in polymeren Multilagen

Task 4.4.1 c) Ablöseprozesse der flexiblen Polymerlagen vom Träger

Task 4.4.1 d) Einbetten in dehnbare Basissubstrate

Task 4.4.1 e) Verbindungstechnologie in dehnbaren Basissubstraten

Task 4.4.1 f) Hochspannungsfestigkeit

Task 4.4.1 g) Testchips

Task 4.5 3D-Verguss für die Herstellung optischer Komponenten

Task 4.5 a) Prozessentwicklung 3D Moldsubstrat

Task 4.5 b) Entwicklung eines Geometrietestvehikels

Task 4.5 c) Entwicklung von Bestückprozessen zur Integration von Funktionselementen

Task 4.5 d) Entwicklung von Direktmetallisierungsprozessen auf Molding Compound

AP5: Aufbau- und Verbindungstechnik (AVT) und Systemintegration

Task 5.2 AVT für Applikation 2 (Kostengünstige Wärmebildgeräte)

Task 5.2.1 Kappenwafer

Task 5.2.2 Vorbereiten Mikrobolometer

Task 5.2.3 Hermetische Verkapselung

Task 5.3 AVT für Applikation 3 (Passive Faserausrichtung für Single-Mode-Transceiver)

Task 5.3.1 Entwicklung eines gemoldeten und metallisierten 3D Substrates angepasst auf den UC 3

Task 5.3.1 a) Entwicklung eines gemoldeten 3D Substrates angepasst auf den UC 3

Task 5.3.1 b) Entwicklung eines Metallisierungsprozesses auf einem 3D Substrat angepasst auf UC 3

Task 5.3.2 3D Montage-Prozess

Task 5.4 AVT für Applikation 4 (Herzüberwachungssystem)

Task: 5.4.1 Flex auf Patch Integration für funktionale Aufbauten

Task 5.4.1 a) Flexible Module mit integrierten Sensoren und ICs

Task 5.4.1 b) Dehnbare funktionale Module

AP6: Testing, Zuverlässigkeit, Fehleranalyse & Messtechnik

Task 6.2 Charakterisierung elektrischer und optischer Eigenschaften

Task 6.3 Qualifikation und Zuverlässigkeit

Task 6.4 Fehleranalyse

AP7: Herstellung und Validierung von Demonstratoren

Task 7.3 Demonstration, Herstellung und Validierung für Applikation 3 (Passive Faserausrichtung für Single-Mode-Transceiver)